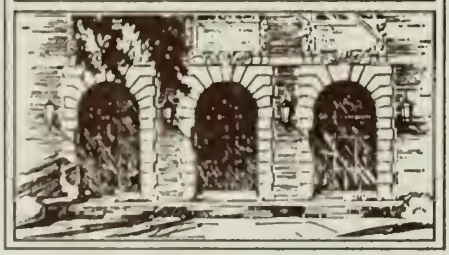

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REPORT NO. 102

APPLICATIONS OF TUNNEL DIODES IN SWITCHING CIRCUITS

by

Toshiro Kunihiro

October 26, 1960

This work was supported in part by the Office of
Naval Research under Contract Nonr-1834(15).

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1. Introduction

The invention of the tunnel diode attracted wide-spread attention among scientists and engineers in the various fields because of its new current-carrying mechanism, i.e., quantum mechanical tunneling. Many people are of the opinion that the fields in which tunnel diodes will show their greatest advantages over other circuit elements are the low noise VHF circuits and the fast switching circuits. In fact, they are found to be very useful in the former field and there are even commercial products using tunnel diodes. Unfortunately, however, the situation in the latter field is far from being advanced. The main difficulty is the lack of directivity in tunnel diodes. Most of the circuits published so far differ from each other only in the way they overcome the difficulty.[1]-[3] All of these circuits, without exception, give directivity to circuits by using a synchronous control pulse, which is basically the same idea as that used in phase-locked oscillator logic. This paper discusses a different approach suggested by Professor W. J. Poppelbaum of the Digital Computer Laboratory of the University of Illinois. It is concluded that directivity will be realized by connecting tunnel diodes with directive elements, especially transistor emitter followers. This philosophy is a natural outcome of the "emitter-follower-diode-logic and common-emitter-switching-amplifier" circuitry on which the new Illinois computer's basic circuits are based. The limiting speed of this (emitter-follower-switching-amplifier) system is that of the switching amplifier. The tunnel diodes are used to replace the slow-speed switching amplifiers in the emitter follower-switching amplifier combination. The author believes that transistor emitter-followers and tunnel diode amplifiers are comparable in speed. The emitter-followers have a two-fold purpose in this system, namely, as directive buffers and at the same time as current amplifiers which will provide logical gain (fanout).

The general considerations for switching circuits in Section 2 may be too obvious to be included. Since they set the foundation of this work and they have not been stated in an explicit form as far as the author knows, they are mentioned in this paper. Sections 3 to 5 describe the methods used to realize the three basic requirements by using tunnel diodes stated in Section 2. In Section 6, a set of basic circuits is presented and some experimental results are given. Other miscellaneous applications are added in Section 7.

2. Basic Requirements for Logical Elements and Logical Circuits

There is a diversity of logical elements and logical circuits which have been known and used to date, such as vacuum tubes, magnetic cores, transistors, diodes, varactors and so forth. There will be even more different types of elements in the future. For this reason, it may be worthwhile to consider the basic requirements that logical elements and logical circuits should satisfy in general. The following three features, (1) gain, (2) directivity, and (3) threshold level, seem, to the author, to be essential and indispensable. We can point out many other requirements, such as reliability, long life, high speed, simplicity and low cost. However, these are not indispensable. Now we will discuss these three basic requirements individually.

2.1 Gain

The necessity of gain is rather obvious. The physical quantity which logical circuits handle and by which information is represented is either magnitude of voltage or magnitude of current. Information may be represented by frequency, by phase, by pulse position, or by pulse width. For instance 0-phase and π-phase in phase-locked oscillators are regarded as two states of bit information "0" and "1", respectively. If we carefully analyze the PLO circuits, we will find that the circuits are not handling phase but voltage, i.e., positive voltage for the 0-phase and negative voltage for the π-phase. The unique feature for the PLO circuits is, as the name indicates, the fact that the phase of the output signal is "locked" to that of the pumping input. In other words, the phase of the positive and negative output pulses is automatically tuned with the phase of the pumping input. Take a magnetic core as another example. A logical "1" may be represented by positive remanent flux $-B_r$ and a logical "0" by negative remanent flux $-B_r$. When a magnetizing field of fixed direction (usually negative direction) is applied to the core, the output voltage or current across the output winding is large for the core storing a "1", but small for the core storing a "0". We will use the output voltage or current as an input to other logical stages. Then the input signals are not remanent flux but voltage (or current).

It is thus clear that in any electronic logical circuit, signals are represented in terms of voltage or current and that the circuits handle the magnitude of voltage or current; we will call the magnitude "signal level".

Since all transmission media have transmission losses, limited bandwidth, and a certain level of noise, and since logical circuits also will have loss, information represented by a signal level will be deteriorated after being transmitted and processed. Therefore, switching circuits must "reshape" it, i.e., re-establish the specified signal level. Gain is necessary. We have used the word "reshape" instead of "amplify". The reason is that information processors do not handle energy and do not require any power gain. An overall gain of unity is necessary and sufficient. Deteriorated input signals are "reshaped" into the normal signal level no matter what the magnitudes of the input levels. All logical circuits currently devised are of this nature. Saturation flux for magnetic cores, saturation and cut-off characteristics for transistors, diode clamping and negative feedback for non-saturating transistor circuits are a few examples.

2.2 Directivity

A circuit may be said to be "directive" if signals appearing at its input terminals change the state of the circuit, while signals appearing at its output terminals do not affect the state of the circuit. In other words, a circuit is "directive" if any change of its state reflects itself at the output terminals but not at the input terminals. Consider a circuit which has three terminals, two input terminals x, y and one output terminal z. If this circuit is not directive, then the state of the circuit is indicated by the signal at the terminal z, but the signal at the terminal affects the state of the circuit in the same way that two input signals do. Furthermore, let us assume that the logical function of the circuit is AND. Then the logical equations governing the signals x, y, z and the state of the circuit f are

$$f = x\, y\, z \tag{1}$$

$$z = f \quad . \tag{2}$$

Equations (1) and (2) are identically satisfied for z = 0. Once the circuit takes the state "0", it cannot change its state. A similarity may be seen for an OR circuit, the logical functions of which are

$$f = x \vee y \vee z \tag{3}$$

$$z = f \quad . \tag{4}$$

Equations (3) and (4) are identically satisfied for z = 1. Once the circuit takes the state "1", no further change of the state is possible. These are exactly the cases for tunnel diode circuits (as explained in Section 5). Without directivity, no combinational circuits can be constructed.

There are several ways to give directivity to circuits:

(1) By applying extra control signals: Suppose we apply a control signal g such that equations (1) and (2) now become

$$f = xyz \vee g \tag{5}$$

$$z = f \tag{6}$$

when g = 1, f = 1 and z = 1. If g is changed to 0, z = f = xy. Therefore a properly timed control signal g can control the direction of information transmission. In this case, g may be considered as a "write pulse". Similarly if we use a control pulse g such that equations (3) and (4) become

$$f = (x \vee y \vee z)\,\bar{g} \tag{7}$$

$$z = f \tag{8}$$

when g = 1, f = 0 and z = 0. If g is changed to 0, z = f = x $\vee$ y. In this case g may be considered as an "erase pulse".

Let us consider the circuit shown in Figure 1 below.

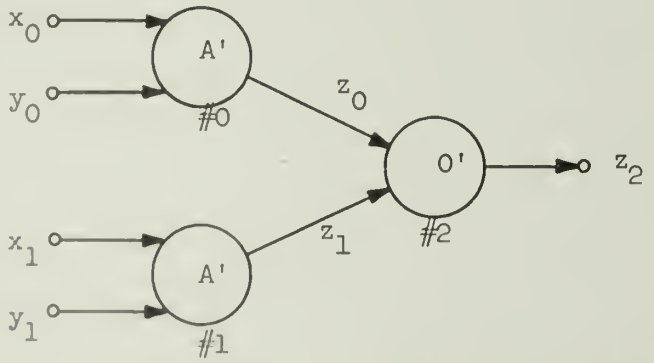


Figure 1. Nondirective Circuit

The logical element A' possesses the logical functions expressed by equations (1) and (2). The logical element O' possesses the logical functions expressed by equations (3) and (4). Then once either f_0 or f_1 (or both) becomes 0 or f_2 becomes 1, the output of the circuit z_2 will not respond correctly to the inputs after that time. However, if we apply a control pulse g as shown in Figure 2, the circuit will become directive. That is, when

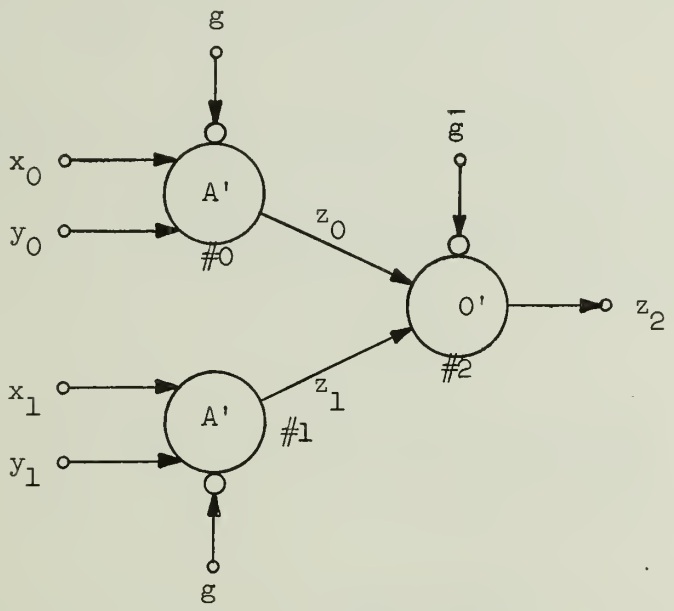
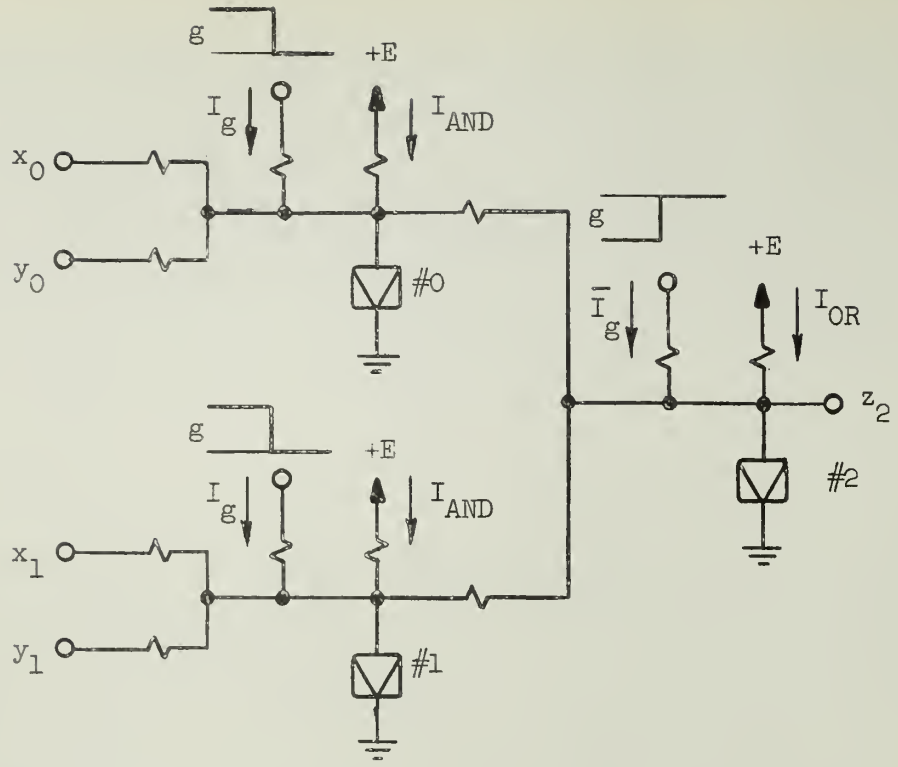


Figure 2. Directive Circuit with Control Pulses

$g = 1$, from equations (5) and (6) $f_0 = z_0 = f_1 = z_1 = 1$ and $f_2 = z_2 = 0$. When g changes to 0, f_0 and f_1 change their states only if either one of their inputs x or y is zero. Therefore z_0 and z_1 correctly represent the logical AND. Similarly only if either z_0 or z_1 (or both) remains 1, z_2 changes from zero to one. Thus $z_2 = x_0y_0 \vee x_1y_1$ if $g = 0$. $\bar{g}$ should be delayed from g by the switching time of A'; otherwise malfunctions will occur. A tunnel diode circuit which embodies the logical circuit of Figure 2 will be shown in Figure 3.

Another more familiar example may be a majority element. Consider a non-directive majority element with three inputs, x, y, and z, and one output u. The output u represents the state of the circuit f but at the same time the output u affects the state in the same way as the three inputs do.



I_{AND} = AND bias current

I_{OR} = OR bias current

= tunnel diode

I_g, $\bar{I}_g$ = control pulse

Figure 3. Tunnel Diode Circuit with Control Pulse

The logical equations are

$$f = M(x, y, z, u) \tag{9}$$

$$u = f \tag{10}$$

where the normal signal levels of x, y, z and u are either +1 or -1.

Consider the change from $x = y = z = 1$ to $x = y = -1$, $z = 1$. If the element is a correct three-input majority element, the output should change from 1 to -1 in response to the input change. However in this case, the new state of the circuit is $f = M(-1, -1, 1, 1)$, i e., the new state is uncertain. However, if we apply a control signal g(0 or 1) such that

$$f = g \times [M(xyzu)] \tag{11}$$

$$u = f \tag{12}$$

where x is algebraic multiplication.

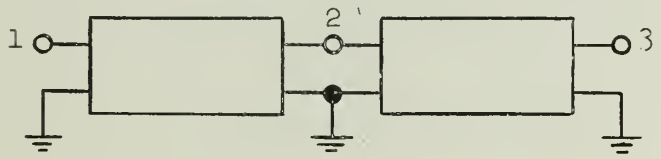
Then

$$f = u = 0 = \text{neutral} \qquad \text{for } g = 0$$

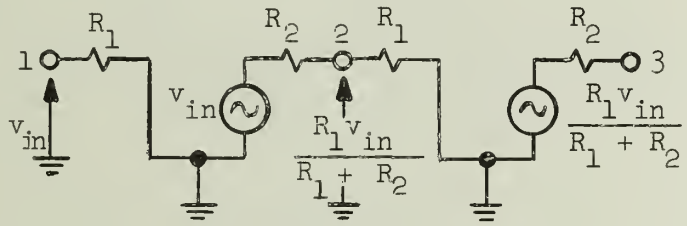
$$f = u = M(x\ y\ z) \qquad \text{for } g = 1 .$$

In practice, the control signal in equation (11) is not of the same nature as the information signals x, y, z and u; rather it will be an excite-release pulse. A PLO circuit with three phase-control pulses is a typical example of this type.

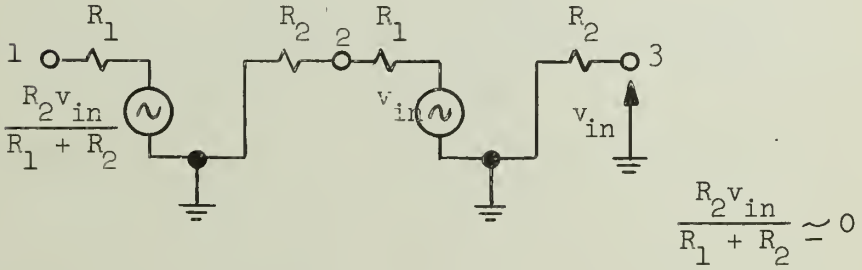
(2) By utilizing the difference of impedance level: Consider a two-port element which has high input impedance R_1, low output impedance R_2 ($R_2 << R_1$) and voltage gain of unity. Signals are represented by voltage levels. As shown in Figure 4, the forward attenuation of the signal is small



(a) Two-port Elements



(b) Forward Transmission

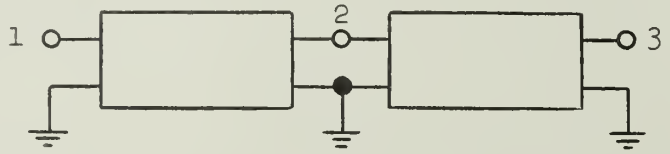


(c) Backward Transmission

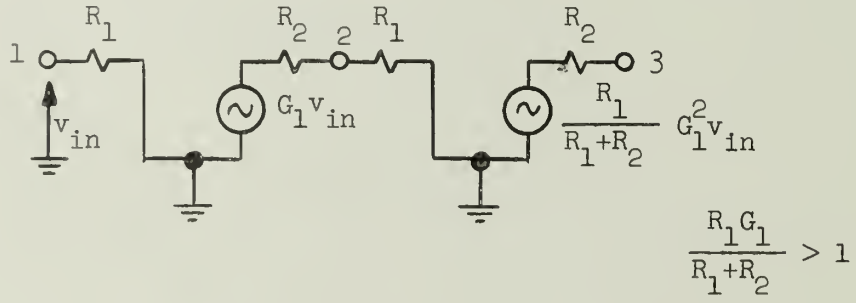
Figure 4. High Input, Low Output Impedance Element

$[R_1/(R_1 + R_2) \simeq 1]$, while the backward attenuation is very high $[R_2/(R_1 + R_2) \simeq 0]$. Hence the element has directivity. Transistor emitter followers have this property. If signals are represented by current levels, then the inverse is true. Namely, the elements which have low input impedance and high output impedance with current gain of unity will have directivity. Common base transistor circuits have this property.

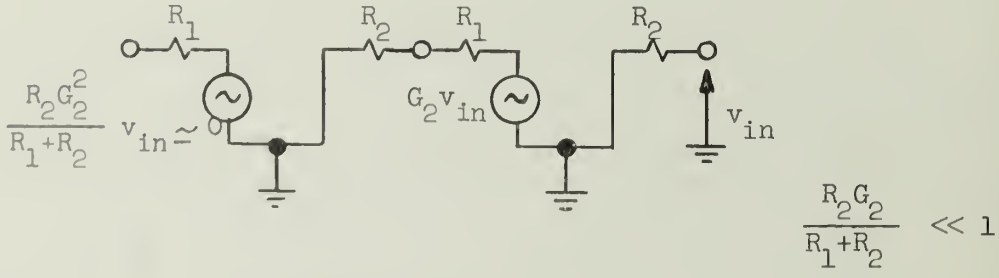
(3) By utilizing the difference of gain: If the forward gain, G_1, of an element is larger than the backward gain, G_2, the element is apparently directive (See Figure 5). Common emitter transistor amplifiers have this property.



(a) Two-port Element



(b) Forward Transmission



(c) Backward Transmission

Figure 5. Element which has Directive Gain

There seems to be a misunderstanding that nonlinear one-port elements (such as diodes) will give directivity. Unfortunately, however, this is not quite true. For instance, the so-called diode logic circuits can be directive only if the following conditions are satisfied.

(a) Output impedances of the incoming signal sources are low, and input impedances of the following circuits to which the outgoing signals are applied are high. Namely, condition (2) is satisfied.

(b) Biasing currents of each stage satisfy the requirements discussed by Yokelson and Ulrich[4]. The requirements are in a sense equivalent to condition (3) because biasing current must be modified by the output currents. This means that damping from the output terminal to the input terminal is required.

The following simple example will demonstrate what we have discussed. Consider a diode logic circuit which realizes the logical functions

$$f_1 = a \vee b$$

$$f_2 = (a \vee b)\, c \qquad (13)$$

$$f_3 = (a \vee b)\, d \quad .$$

The logical circuit which realizes equation (13) is shown in Figure 6. AND and OR are embodied using ideal diodes as shown in Figure 7.

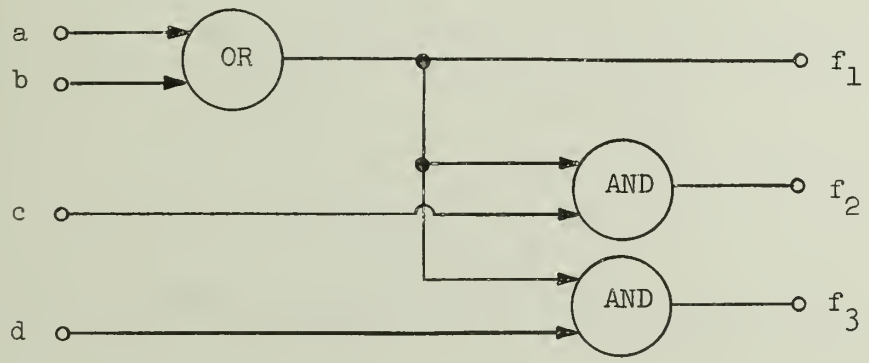
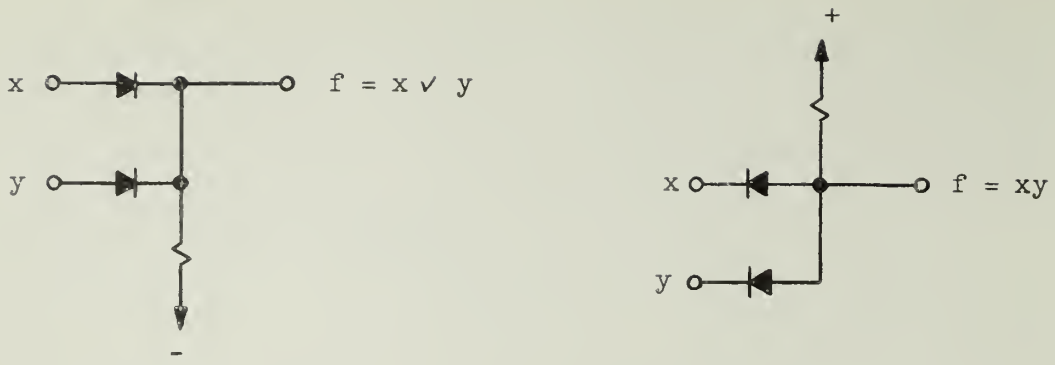


Figure 6. Logical Circuit which Realizes Logical Functions (13)



OR Circuit AND Circuit

Figure 7. Diode Logic

In order to realize the logical circuit shown in Figure 6, the diode logic circuits in Figure 7 are interconnected as shown in Figure 8.

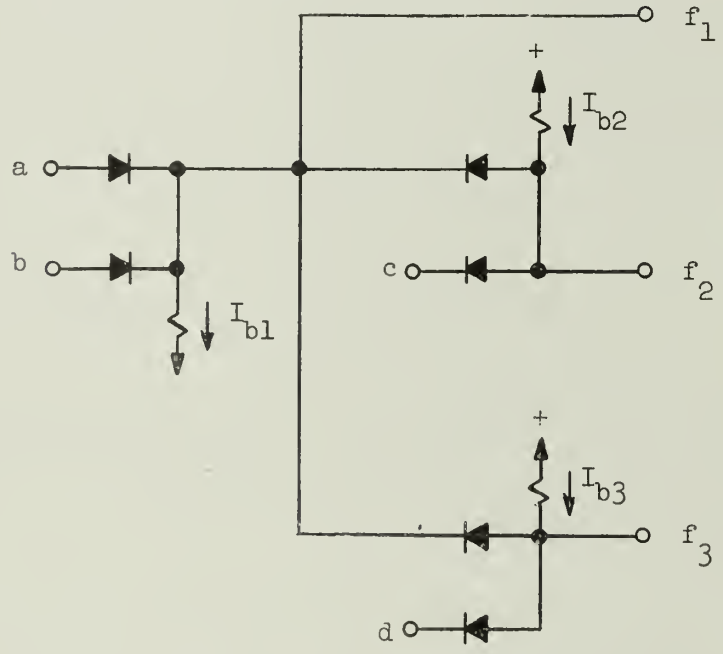
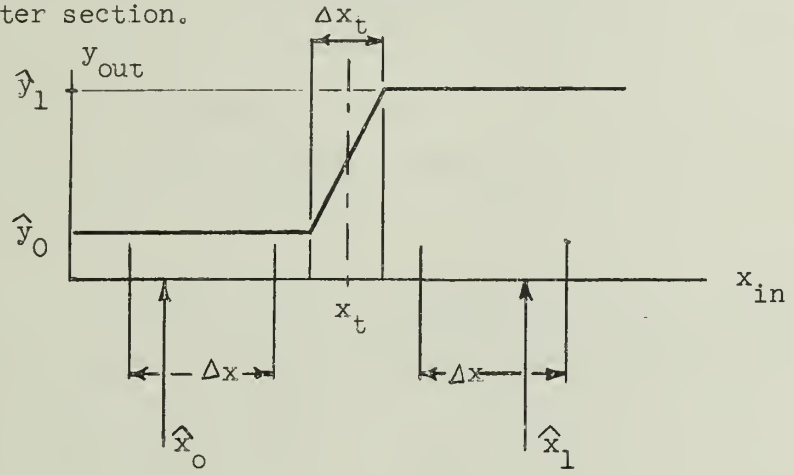


Figure 8. Diode Logic which is Supposed to Realize the Logical Functions (13).

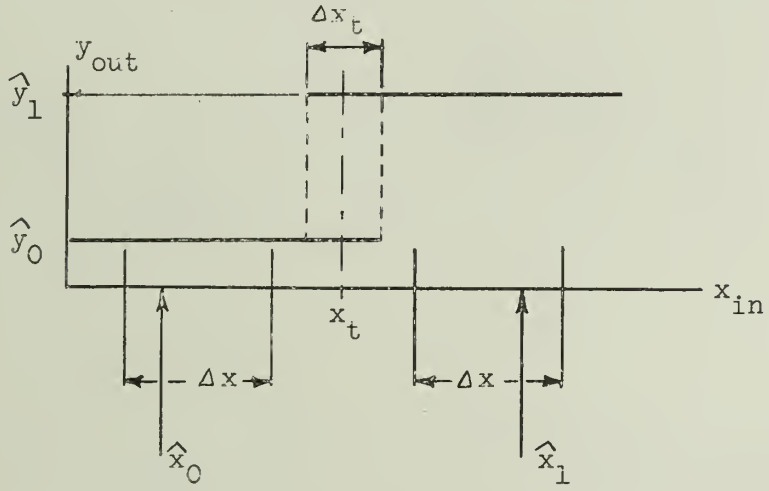
However the circuit will fail to function correctly. Suppose a = b = 0, c = d = 1. Then f_1, f_2 and f_3 will be 1 instead of 0, unless the bias condition $I_{b1} > I_{b2} + I_{b3}$ holds. Namely, there are feedback loops from the output terminals of AND circuits to their input terminals.

2.3 Threshold Level

The threshold level will be defined as the input signal level, x_t, at which the gain of the switching circuit changes sharply. The sensitivity, Δx_t, will be defined as the range of the input signal levels near the threshold level such that if the input signal levels exceed this range, the output signal levels are at the nominal level or in the bands which fall on the favorable sides of the nominal levels. As shown in Figure 9, it does not matter whether the gain of the circuit at the threshold level is degenerative or regenerative. Each has its unique advantages, as will be discussed more thoroughly in a later section.



(a) Without Hysteresis Loop



(b) With Hysteresis Loop

$\hat{x}_0$, $\hat{y}_0$ and $\hat{x}_1$, $\hat{y}_1$ are nominal signal levels for "0" and "1", respectively. Δx is the range within which signals may be deteriorated after being transmitted and processed.

Figure 9. Threshold Level x_t and Sensitivity Δx_t

Although the requirements for switching circuits to reshape signal waves is the primary reason that the threshold level is necessary, there is another reason for it. A signal level must be allowed to spread within its allowed band, because circuit components and power supplies are subject to inevitable natural tolerances and because a certain degree of level shifting during transmission and processing is unavoidable. Then the change of signal levels within their allowed bands should not cause any change of the state of the circuit to which the signals are impressed. This requirement and the requirement of having enough gain to reshape the waveforms can be compatible only if there is a threshold level in the input signal level to the circuit.

Sensitivity will determine the fan-in to the circuit. Higher sensitivity is desirable for any case. Considerations of noise will influence the selection of the nominal levels of signals but it will not affect the sensitivity.

In connection with the threshold level, methods to combine inputs will be discussed here. There are two ways, i.e., linear combination and non-linear combinations. Resistor logic and magnetic core logic (see Figure 10) are examples of the linear combination. The resultant input is proportional to the algebraic sum of input signals.

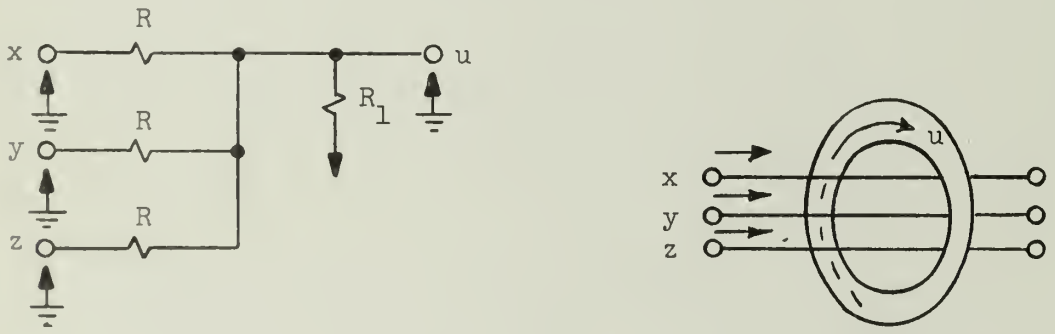
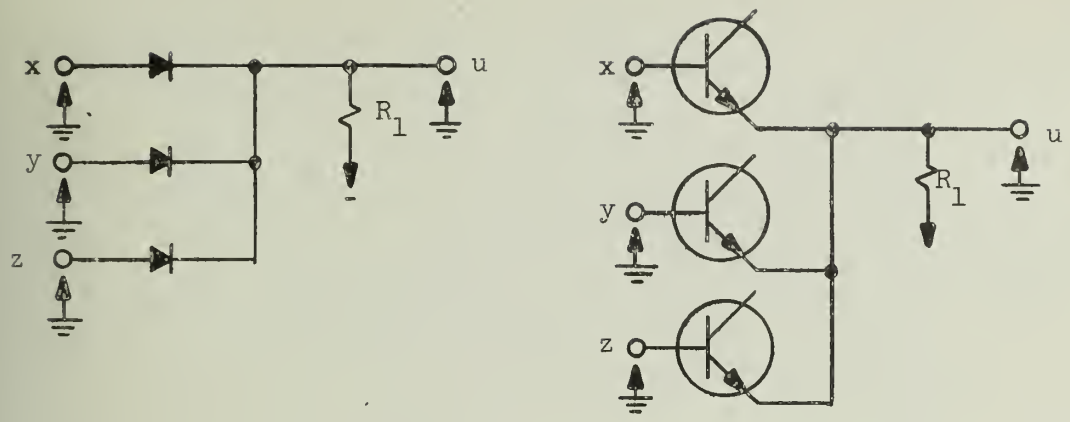


Figure 10. Linear Combination of Inputs

Diode logic and DCTL (direct-coupled transistor logic) are examples of the nonlinear combination (see Figure 11).



$$u = \mathrm{Max}(x, y, z)$$

Figure 11. Nonlinear Combination of Inputs

It is interesting to see that all logical elements with linearly combined inputs are majority (or minority) decision elements. Because of preset biases, such as bias current in resistor logic and coercive magnetic force in cores, this fact is often disguised. If we realize that these biases are constant input signals, the function of the circuits is merely the majority function (or the minority function if the gain of the circuit is negative). The circuits with nonlinearly combined inputs do not have this feature, rather their functions are comparison functions.

So far we have been discussing the basic requirements which any logical elements and logical circuits should fulfill. In the following sections, we will discuss the methods to embody these logic requirements using tunnel diodes.

3. Threshold Level of Tunnel Diodes

Before going into this subject, the characteristics of tunnel diodes will be remarked upon briefly. The notations used in Figure 12 are taken from I. A. Lesk et. al.[5]. A complete physical explanation of the characteristics is beyond the scope of this paper. The reader may refer to many articles which have been published up to now.[5]-[8]. The measured characteristic of several sample diodes are shown in Figure 13. The peak current I_p is proportional to

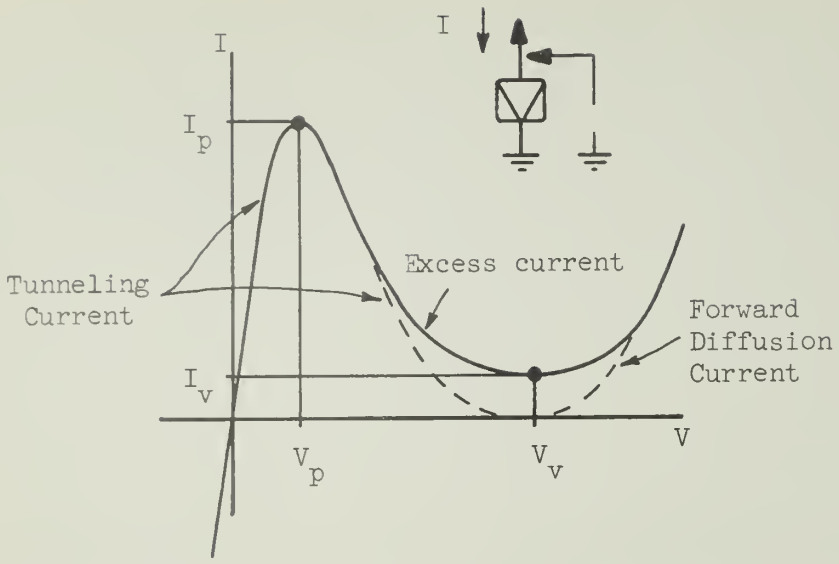
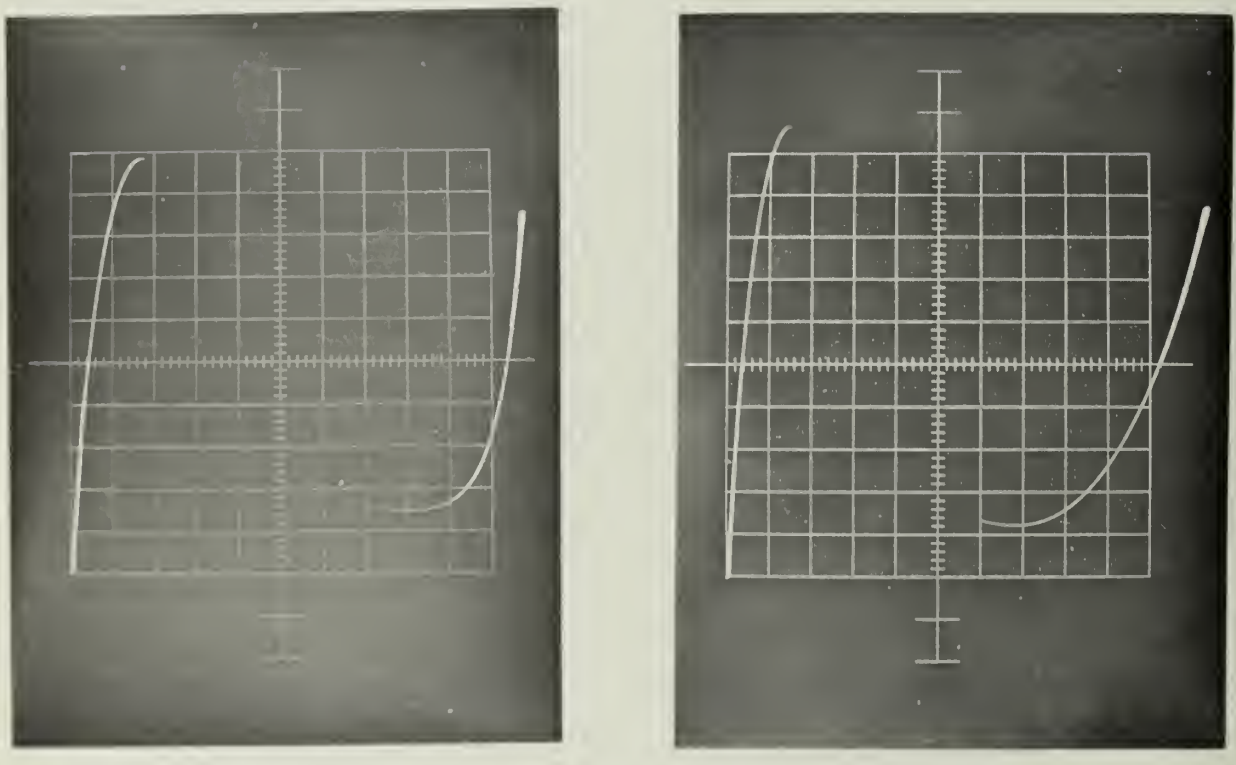


Figure 12. Tunnel Diode V-I Characteristics



0.1 ma/div ⟷ 0.05 v/div

(a) Germanium

0.5 ma ⟷ 0.1 v

(b) Gallium Arsenide

Figure 13. Measured Characteristic of Tunnel Diodes

the junction area. In commercially available tunnel diodes, the peak voltage, V_p, and the valley voltage, V_v, are nearly constant for material. Germanium gives a valley voltage of about 0.3 v, silicon 0.45 v, and gallium-arsenide 0.75 v.

The threshold level of tunnel diodes is related to I_p and I_v. Usually the peak is sharp, but the valley is flat. If a single diode is used, the input-output characteristic is rather poor as shown in Figure 14. The poor threshold characteristic is caused by the flat valley.

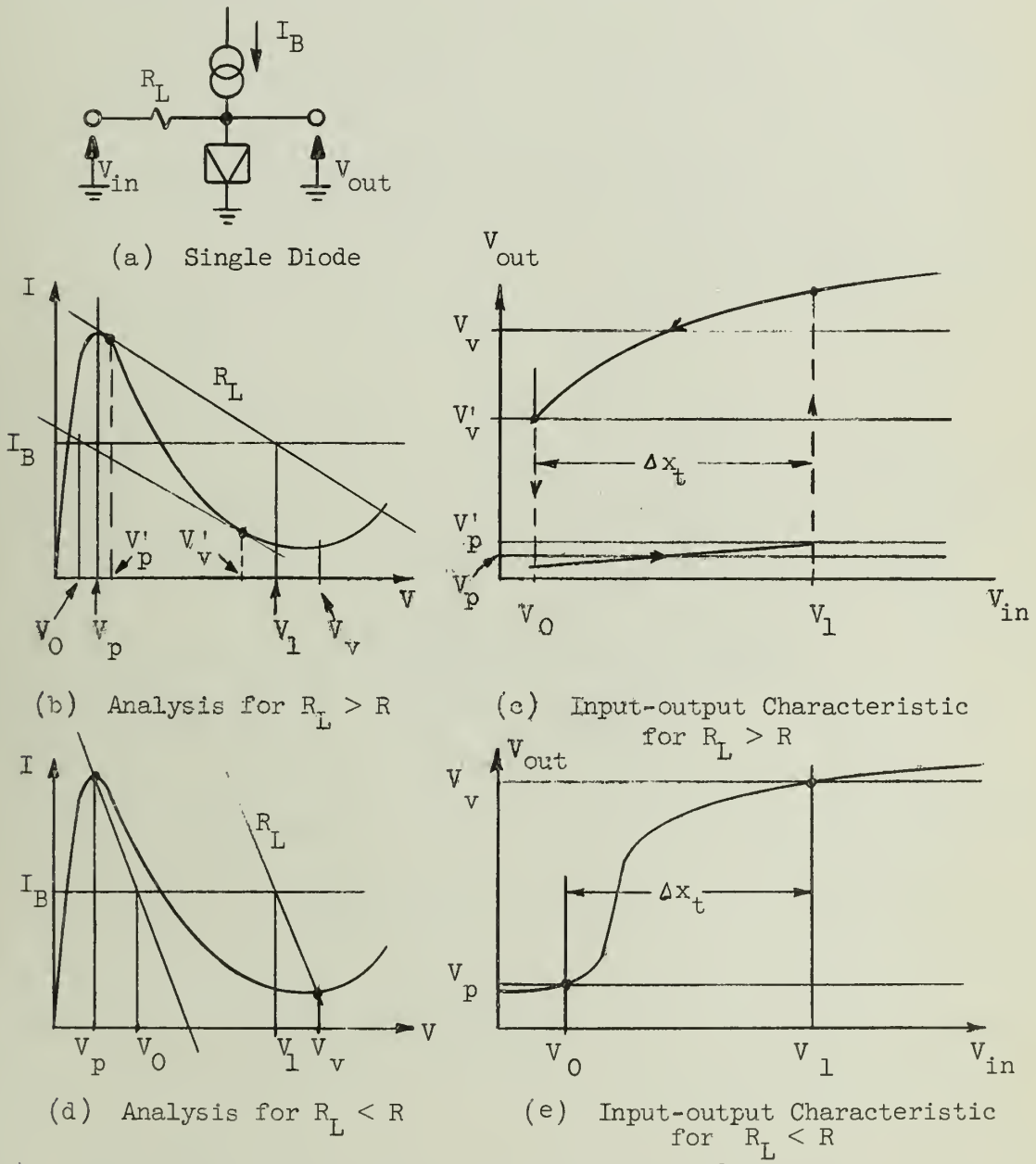
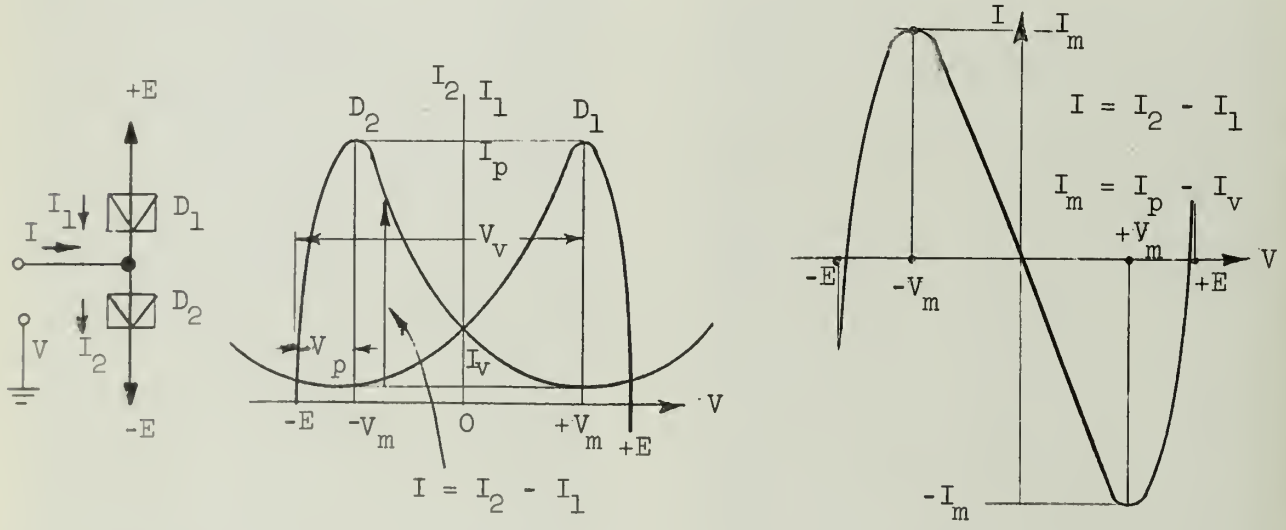


Figure 14. Input-output Characteristic of a Single Diode
(R is the absolute value of negative resistance)

For the circuit in which the load resistance, R_L, is larger than the absolute value of the negative resistance R, the upper threshold level V_1 is fairly well controlled because the point comes from the sharp peak. Therefore if only V_1 is utilized as a threshold level and a large enough reset control pulse is applied, the flat threshold level V_o does not affect the performance of the circuit. This scheme is one of the common methods used to construct logical circuits using tunnel diodes. However, this automatically means that the system is synchronous and requires high speed, and high power control pulses. Since any synchronous system seems to have difficulties in high-speed operations and since the complexity of synchronization will be more serious than the complexity due to asynchronism, no synchronized pulse control is desirable. Rather two (forward and backward) sharp threshold levels are favorable. An immediate solution in order to realize two sharp peaks is to use two tunnel diodes in the form of a "diode pair" as shown in Fig. 15.



(a) Diode Pair (b) Analysis (c) Characteristic of Diode Pair

Figure 15. Diode Pair

In order to minimize the variation due to the variation of bias voltages +E and -E, E should be equal to $(V_p + V_v)/2$. Then the peak current I_m is equal to $I_p - I_v$.

A diode pair has many advantages over a single diode:

(a) Sharp threshold levels for both directions;

(b) Wider linear negative resistance region, which is important to increasing sensitivity. Since even order nonlinear terms of the negative resistance vs. the voltage characteristic curve are cancelled out in diode pairs, the linear term will be extended to a wider voltage range in diode pairs than in single diodes;

(c) Characteristics are symmetric with respect to the neutral point. This will simplify the detailed analysis of circuits;

(d) Output signal levels can be balanced with respect to the ground (equal magnitude and opposite sign).

Using diode pairs, the bilateral sharp threshold level will be obtained. Theoretically the sensitivity can be infinite (Δx_t in Figure 9 can be zero). Further arguments will be found in the following sections.

4. Wave Shapers using Tunnel Diodes

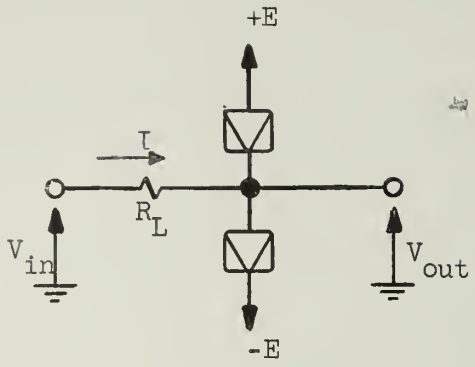
In this section, several wave shapers which accomplish one of the basic requirements discussed in Section 2 will be discussed. These wave shapers are the key circuits in tunnel diode circuitry described in this paper.

4.1 Voltage Wave Shaper with Positive Gain - Restorer

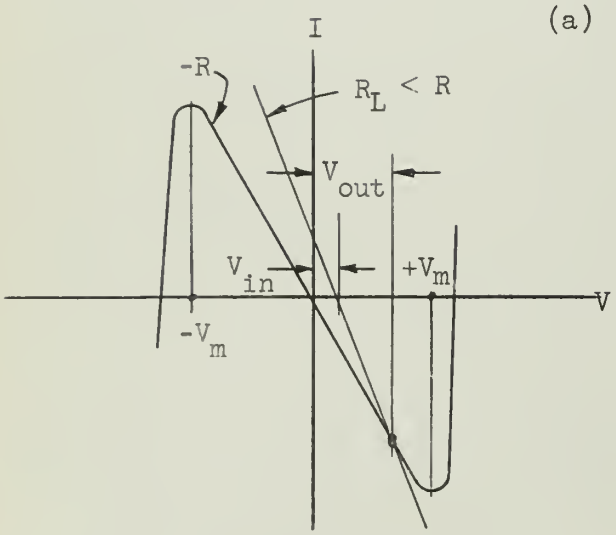
Utilizing the negative resistance, high gain will be obtained. The threshold level will give shaping action. There are two voltage wave shapers; one has positive gain and the other negative gain. The former will be described in this subsection. Figure 16 shows the circuit and its graphical analysis.

The dc gain, G_o, at the threshold level, i.e., at the zero input voltage is

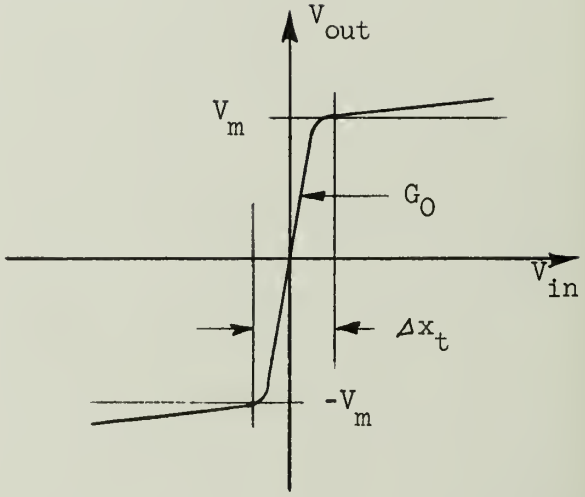
$$G_o \cong \frac{R}{|R_L - R|} \quad . \tag{14}$$



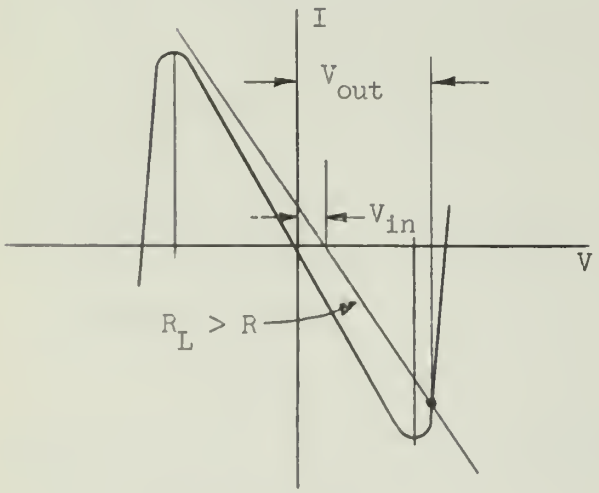
(a) Restorer



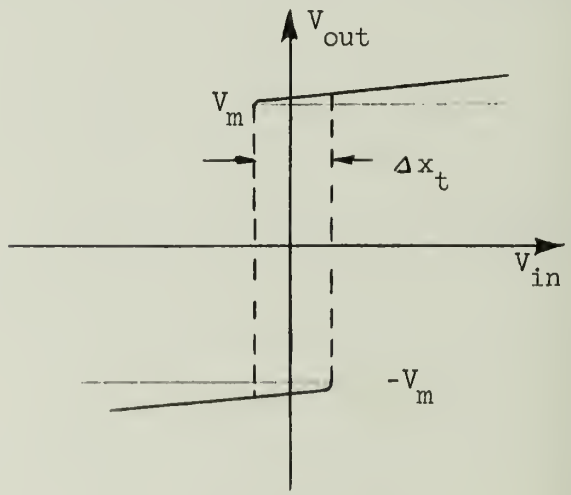
(b) Analysis for $R_L < R$



(c) Input-output Characteristic for $R_L < R$



(d) Analysis for $R_L > R$



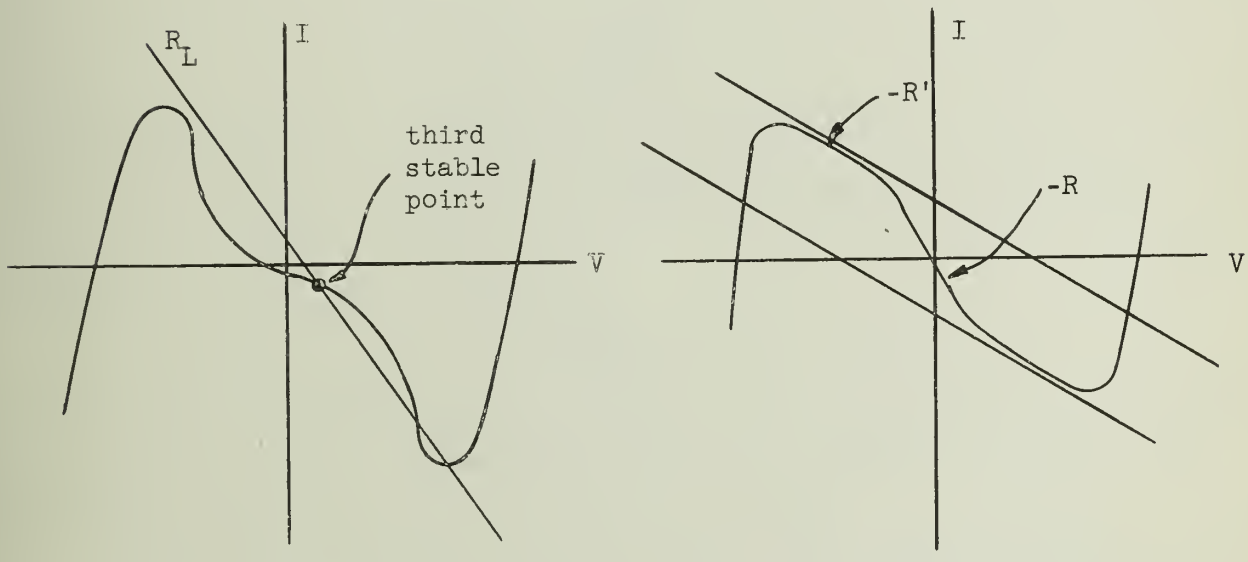
(e) Input-output Characteristic for $R_L > R$

Figure 16. Restorer

G_o can be infinite if $R_L = R$. However this condition seems to be impossible to realize, because

(1) both R_L and R are subject to variation due to commercial tolerance, bias voltage variation and nonuniformity of tunnel diode characteristics among samples,

(2) nonlinearity of negative resistance in the negative resistance region (see Figure 17). In case (a) in Figure 17, if the load resistance R_L is too small there is a third stable point. To avoid this R_L should be larger than the average R. Hence we cannot realize $R_L = R$. A similar argument holds for case (b). During experiments, it was found that case (a) was a rather annoying factor which degraded the performance of the circuit. To eliminate this, the bias voltage E should be lowered. This in turn lowers the signal levels and tends to make circuits unstable. GaAs tunnel diodes seem to be unsuitable in this respect.

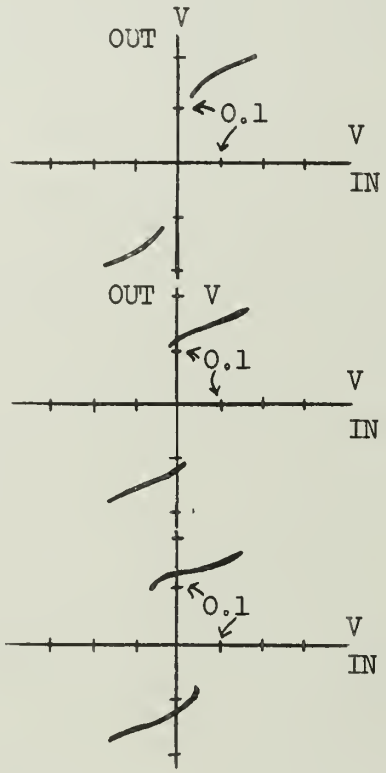


(a) Third-order Harmonics with Negative Coefficient

(b) Third-order Harmonics with Positive Coefficient

Figure 17. Nonlinearity in Negative Resistance Region

The measured results using germanium tunnel diodes (GE) are shown in Figure 18. The circuit will not possess a hysteresis loop if R_L is smaller than R. If, however, R_L is too much smaller than R, the circuit tends to oscillate. If R_L is too large, the width of the hysteresis becomes large and the circuit loses sensitivity.



$R_L = 120\,\Omega$

$R_L = 160\,\Omega$

$R_L = 220\,\Omega$

$R \cong 160\,\Omega$

Figure 18. Restorer (measured)

The switching speed of the restorers is directly related to the RC product of tunnel diodes if the leakage inductance of the diodes is neglected. The response during transition to the step input V_{in} is

$$\frac{V_{out}}{V_{in}} = \frac{R}{R_L - R}\left(e^{(R_L-R)t/RCR_L} - 1\right) \simeq \frac{t}{R_L C} \qquad (15)$$

where C = transition capacitance of the junction.

In asynchronous circuitry, R_L is designed to be closely equal to R. Then equation (15) becomes

$$\frac{V_{out}}{V_{in}} \simeq \frac{t}{RC} = \frac{t}{T}$$

or

$$t/\frac{V_{out}}{V_{in}} = \frac{t}{G} = T \quad . \tag{16}$$

That is, the inverse gain bandwidth t/G is constant and equal to the RC product of the tunnel diode. The leakage inductance, L_S, will increase the time constant T in Equation (16), such that

$$T' \simeq T + T_S \quad \frac{1}{G_o} \tag{17}$$

where

$$T_S = \frac{L_S}{R}$$

$$G_o = \frac{R}{|R_L - R|} \quad .$$

Since tunnel diode circuits are generally low impedance circuits, $T_S = L_S/R$ will not be neglibible even for the leakage inductance of carefully designed tunnel diodes. High gain seems to reduce the effect of the leakage inductance. More exact analysis will be reported separately.

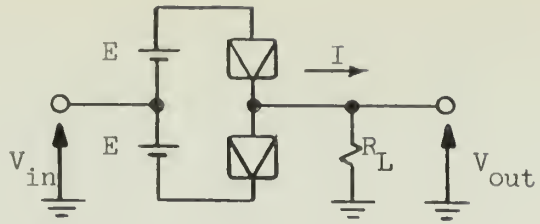
4.2 Voltage Wave Shaper with Negative Gain - Invertor

The circuit and its graphical analysis are given in Figure 19. Voltages shown by an arrow pointing from right to left in this figure are negative. The arrows pointing from left to right show positive voltages.

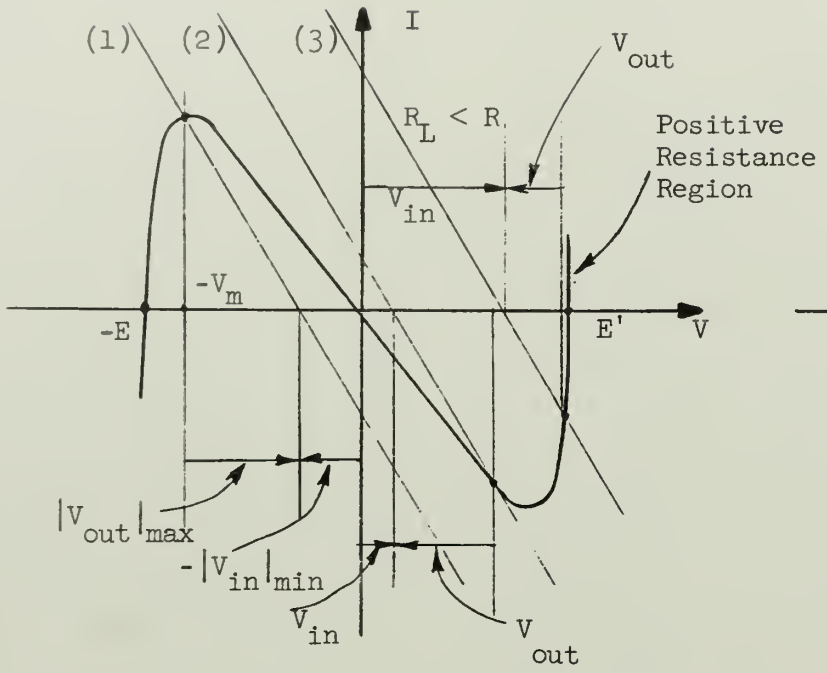
The relationship between $|V_{out}|_{max}$ and $|V_{in}|_{min}$ is

$$|V_{out}|_{max} + |V_{in}|_{max} = V_m$$

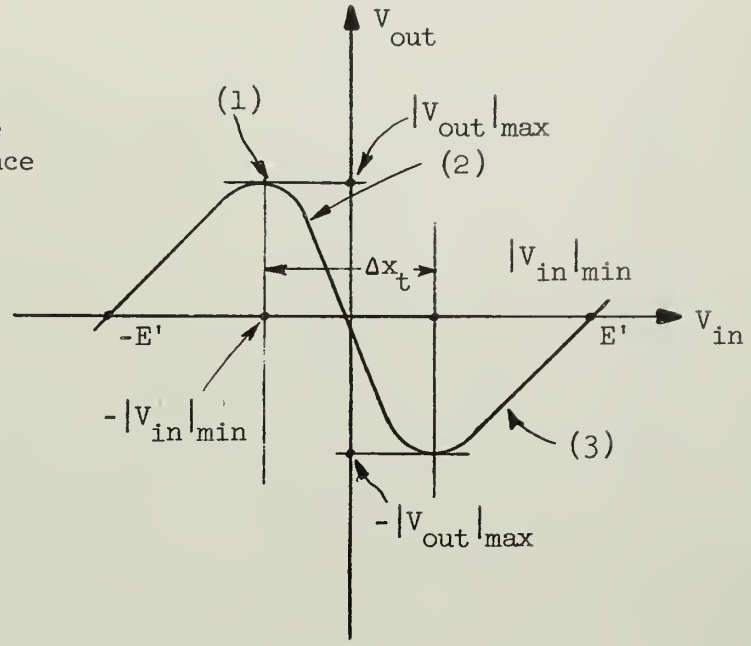
$$\frac{|V_{out}|_{max}}{|V_{in}|_{min}} = \frac{R_L}{R - R_L} = G_o \qquad \text{for } R_L < R$$



(a) Inverter

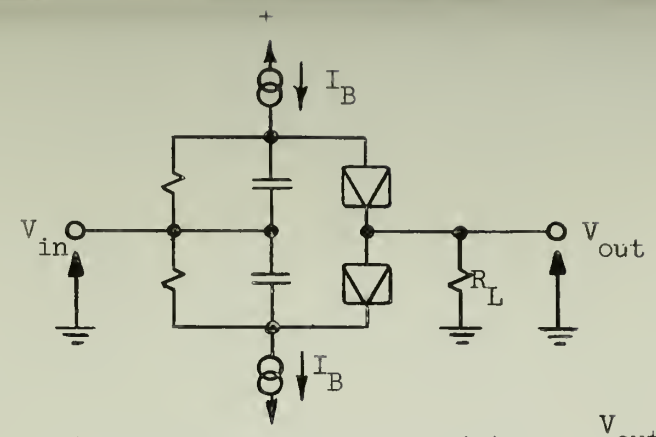


(b) Analysis for $R_L < R$

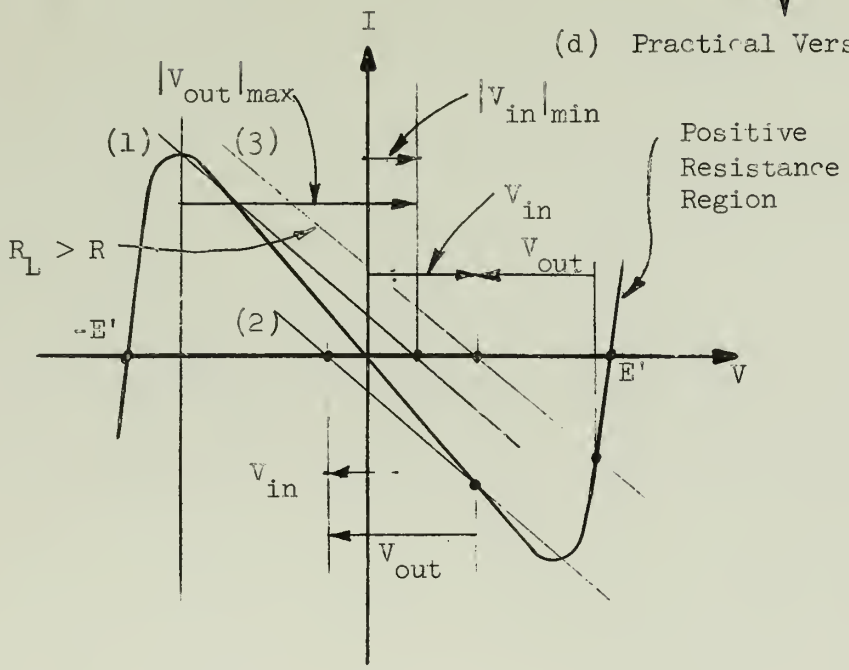


(c) Input-output Characteristic for $R_L < R$

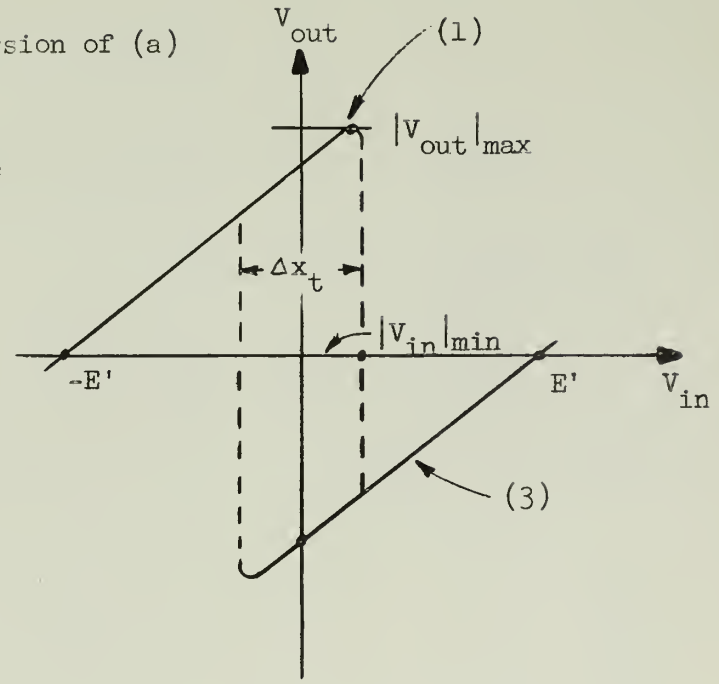
Figure 19. Inverter



(d) Practical Version of (a)



(e) Analysis for $R_L > R$



(f) Input-output Characteristic for $R_L > R$

Figure 19 (Continued). Inverter

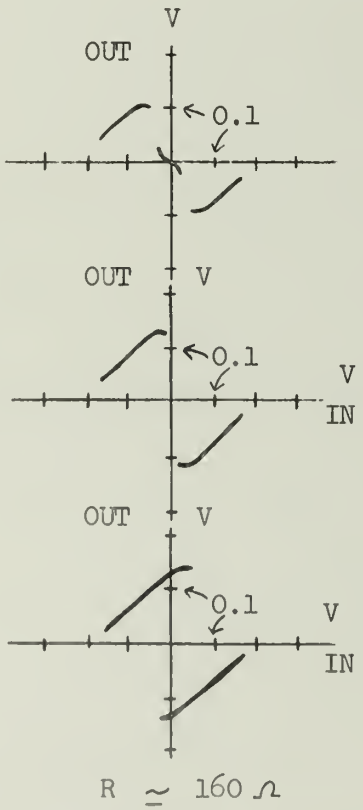
$$\left.\begin{aligned} |V_{out}|_{max} - |V_{in}|_{min} &= V_m \\ \frac{|V_{out}|_{max}}{|V_{in}|_{min}} &= \frac{R_L}{R_L - R} = G_o \end{aligned}\right\} \quad \text{for } R_L > R \ .$$

$|V_{out}|_{max}$ increases as R_L increases. When the load line intersects the positive resistance region as shown by (3) in Figure 19, there are relations

$$V_{in} - V_{out} \cong \frac{1}{2}(E' + V_m) \qquad \text{for } V_{in} > 0$$

$$V_{in} - V_{out} \cong -\frac{1}{2}(E' + V_m) \qquad \text{for } V_{in} < 0 \ .$$

Therefore the output voltage decreases sharply after the load line passes over the peak points. A limiter which limits the excess swing of the input signal may be necessary in order to maintain the required output level. However, this in turn slows down the switching speed of the inverter. For this reason two-wire logic is preferable.



$R_L = 120\Omega$

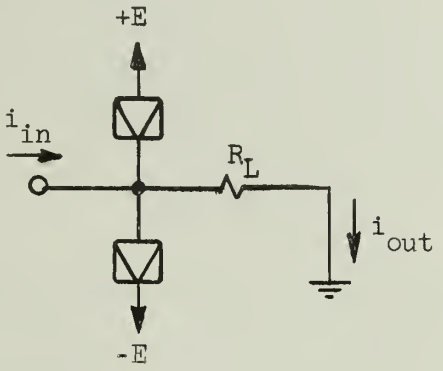
$R_L = 160\Omega$

$R_L = 220\Omega$

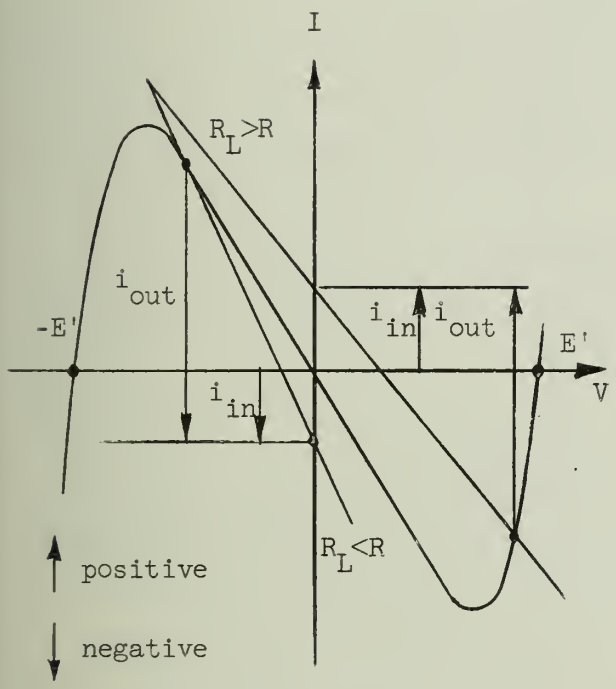
Figure 20. Inverter (measured)

4.3 Current Wave Shaper - Current Restorer

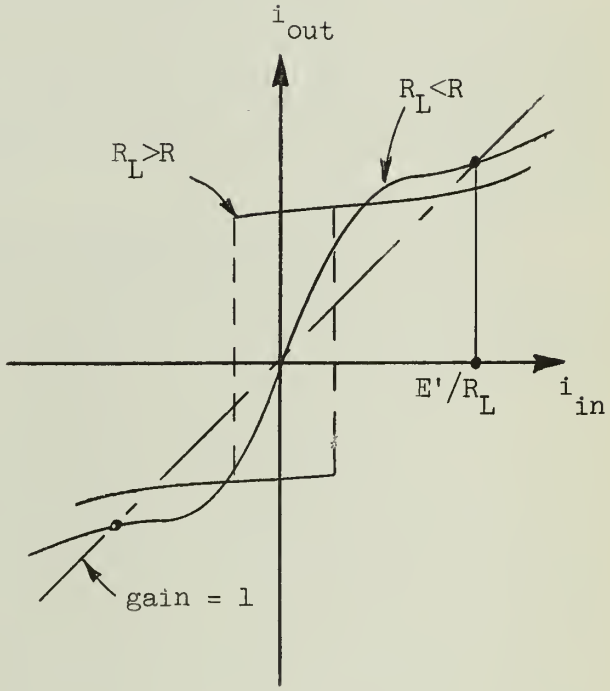
Figure 21 shows the circuit and its graphical analysis of a current restorer.



(a) Current Restorer



(b) Graphical Analysis



(c) Input-output Characteristic

Figure 21. Current Restorer

The dc current gain is

$$G_o \cong \frac{R}{|R_L - R|} \quad , \tag{18}$$

which is the same as the voltage restorer. The input impedance of the following stage after current restorers should be low. The switching speed also is the same.

5. Emitter Follower as a Directive Coupler

Among three possible ways to obtain directivity, the first scheme, which uses control pulses, will lead to a synchronous system which is less interesting. By generating control pulses at each stage, an asynchronous system may be constructed. However, high power control pulse generators are required at each stage and the switching speed of the system will be limited by the speed of the generators. The third scheme, which uses common emitter amplifiers, is not suitable in tunnel diode circuitry because

(a) switching speed of common emitter amplifiers is rather slow and has a considerable delay time;

(b) tunnel diodes work as a perfect wave shaper and no more gain is needed in the system.

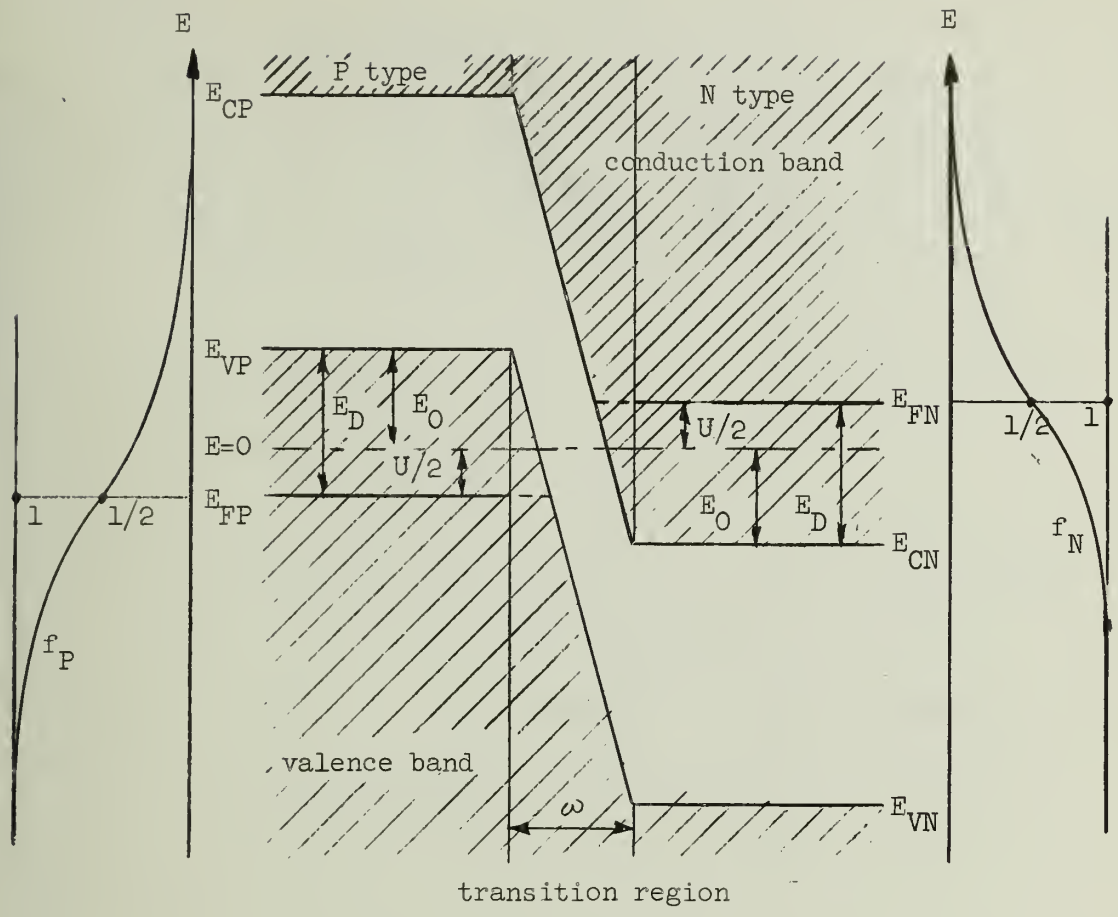
For some cases, e.g., when signal levels of a tunnel diode system must be converted into signals of other systems, common emitter amplifiers may be used, but this is not a general case. Thus, the only choice is the second scheme in which emitter-followers are used.

Which is slower--a tunnel diode wave shaper or an emitter follower? To answer this interesting question, the inverse gain-band-width of both tunnel diodes and emitter followers will be compared next.

5.1 Inverse Gain-Band-Width of Tunnel Diodes

5.1.1 Analysis of tunneling current applying energy band theory: As derived in equation (16), the inverse gain-band-width of a tunnel diode is its RC product. Assuming that the degeneracies of both P-type and N-type semiconductors are the same, i.e., the junction is symmetric, the RC product will be calculated below. The energy band configuration is shown schematically in Figure 22. The assumed properties of the junction are shown in Figure 23.

Consider the transition of electrons between an infinitesimal volume dv_p in the P-side and an infinitesimal volume dv_n in the N-side at energy level E due to quantum mechanical tunneling.



E_{CP}, E_{CN} = conduction band edges of P-type and N-type semiconductors

E_{VP}, E_{VN} = valence band edge of P-type and N-type semiconductors

E_{FP}, E_{FN} = Fermi level of P-type and N-type semiconductors at thermal equilibrium

E_G = forbidden energy gap = $E_{CP} - E_{VP} = E_{CN} - E_{VN}$

E_D = $E_{VP} - E_{FP} = E_{FN} - E_{CN}$ = degeneracy

U = eV, where V: forward voltage applied across the transition region.

f_P, f_N = Fermi Dirac functions for P-type and N-type semiconductors

Figure 22. Schematic Energy Diagram of Degenerate PN Junction

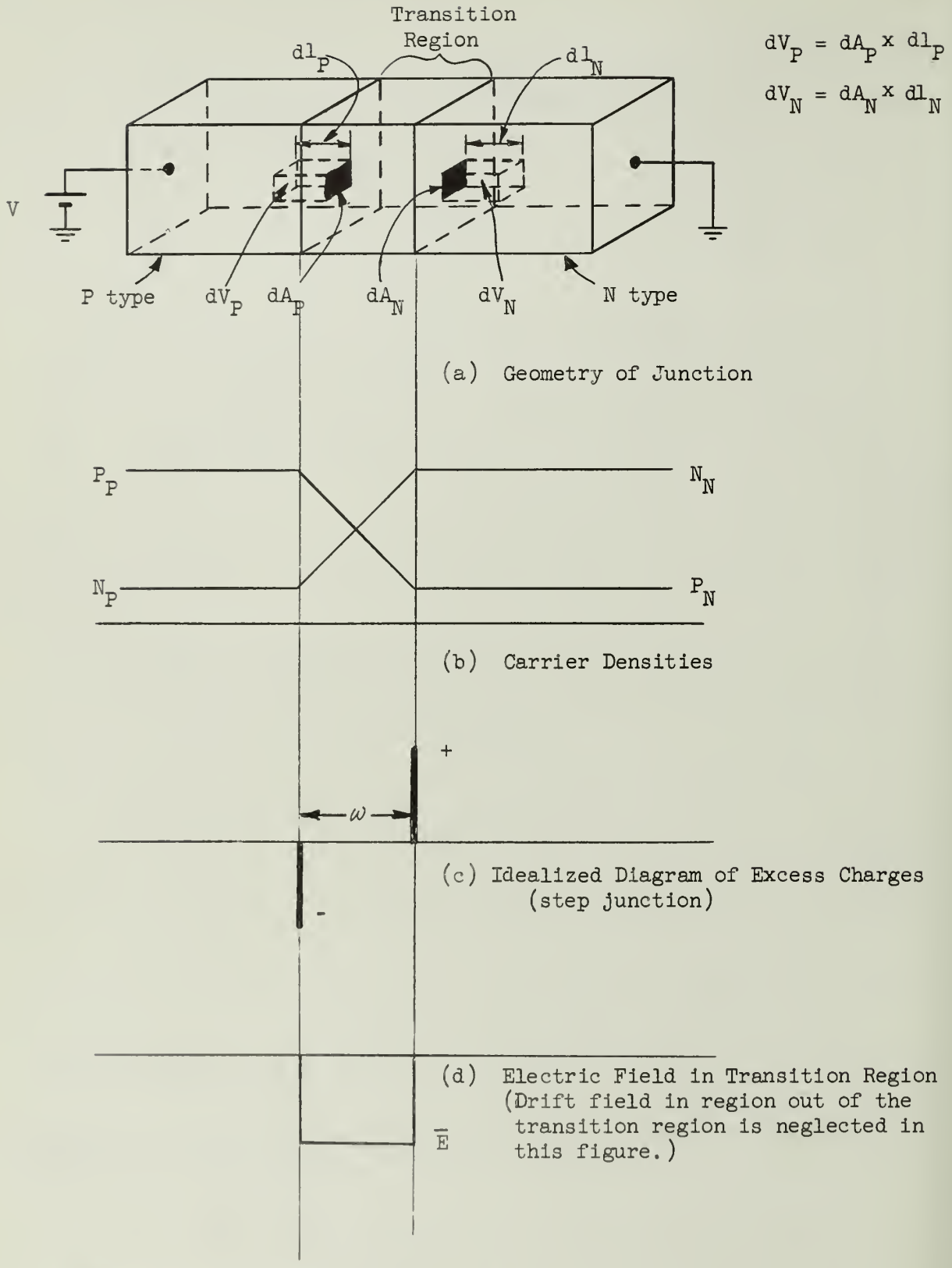


Figure 23. Assumed Properties of Junction

$di_{P\to N}$ = electron flow from dv_P to dv_N

$$= (dn_P)(dn'_N)Z_{P\to N} \tag{19}$$

$di_{N\to P}$ = electron flow from dv_N to dv_P

$$= (dn'_P)(dn_N)Z_{N\to P} \tag{20}$$

where

dn_P and dn_N = number of electrons in dv_P and dv_N, respectively;

dn'_P and dn'_N = number of vacant states available for electrons in dv_P and dv_N respectively;

$Z_{P\to N}$ = probability per unit time, i.e., the rate at whcih electrons can tunnel from dv_P to dv_N through the transition region under an electric field;

$Z_{N\to P}$ = the same as $Z_{P\to N}$ except reversed direction.

di = net electric current from dv_P to dv_N carried by $di_{P\to N}$ and $di_{N\to P}$

$$= e(di_{N\to P} - di_{P\to N}) \quad . \tag{21}$$

From the quantum mechanical theory, we get

$$dn_P = dv_P \cdot 4\pi\left(\frac{2m_{eff}}{h^2}\right)^{3/2} (E_{VP} - E)^{1/2}\, dE \cdot f_P \tag{22}$$

$$dn'_P = dv_P \cdot 4\pi\left(\frac{2m_{eff}}{h^2}\right)^{3/2} \left(E_{VP} - E\right)^{1/2} dE(1 - f_P) \tag{23}$$

$$dn_N = dv_N \cdot 4\pi\left(\frac{2m_{eff}}{h^2}\right)^{3/2} \left(E - E_{CN}\right)^{1/2} dE \cdot f_N \tag{24}$$

$$dn'_N = dv_N \cdot 4\pi\left(\frac{2m_{eff}}{h^2}\right)^{3/2} \left(E - E_{CN}\right)^{1/2} dE(1 - f_N) \tag{25}$$

$$f_P = \frac{1}{1 + e^{(E-E_{FP})/kT}} \tag{26}$$

$$f_N = \frac{1}{1 + e^{(E-E_{FN})/kT}} \tag{27}$$

$$Z_{P\to N} = \frac{1}{\tau_P} P_{P\to N} \tag{28}$$

$$Z_{N\to P} = \frac{1}{\tau_N} P_{N\to P} \tag{29}$$

where

$P_{P\to N}$ is the transmission probability of the electron through the transition region from the P side to the N side;

$P_{N\to P}$ is the transmission probability of the electron through the transition region from the N side to the P side;

τ_P is the time interval of successive strikings of the electron at the P side of the transition region;

τ_N is the time interval of successive strikings of the electron at the N side of the transition region.

We assume that

$$P_{P\to N} = P_{N\to P} = \exp\left[-\frac{4}{3}\frac{\sqrt{2m_{eff}}}{\hbar e \bar{E}} (E_G)^{3/2}\right] \triangleq P \tag{30}$$

$$\tau_P = \tau_N = \frac{h}{ae} \triangleq \tau \tag{31}$$

where

a = crystal lattice parameter.

Utilizing these relations, equation (21) will become

$$di = e\frac{P}{\tau}(4\pi)^2\left(\frac{2m_{eff}}{h^2}\right)^3 \sqrt{(E_{VP} - E)(E' - E_{CN})}\,(f_N - f_V)\,dE dE' dv_P dv_N \tag{32}$$

Therefore the total tunneling current is

$$I = e(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \int_{\text{related volume}} dv_P dv_N \int_{E_{CN}}^{E_{VP}} \int_{E_{CN}}^{E_{VP}} \frac{P}{\tau} \sqrt{(E_{VP} - E)(E' - E_{CN})}$$

$$\cdot (f_N - f_V)\, dE dE'$$

$$= e(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \int_{\text{related volume}} dl_P dl_N dA_P dA_N \int_{E_{CN}}^{E_{VP}} \int_{E_{CN}}^{E_{VP}} \frac{P}{\tau} \sqrt{(E_{VP} - E)(E' - E_{CN})}$$

$$\cdot (f_N - f_V)\, dE dE' \qquad (33)$$

Now let us consider dl_P and dl_N in the integration (33). Since we assumed the carrier densities outside of the transition region are in the steady state (see Figure 23(b)), the current outside of the region must be the drift current with the drift velocity $(v_d)_P$ for the P side and $(v_d)_N$ for the N side. Therefore, during the interval of successive strikes, τ, the electron travels $(v_d)_P \tau$ for the P side and $(v_d)_N \tau$ for the N side. Namely, the electrons located in the volume $(dA_P)\cdot(v_d)_P$ and in the $(dA_N)\cdot(v_d)_N$ must be providing the sources for tunneling electrons. Hence, we substitute $(v_d)_P$ and $(v_d)_N$ for dl_P and dl_N. Since the tunneling probability P is defined at the same energy level for both the P side and the N side, P is zero if $E \neq E'$. Furthermore, the tunneling is possible only along the electric field. Therefore, P = 0 if dA_P and dA_N are not on the same longitudinal line which is in the same direction as the electric field. Thus finally we will derive

$$I = e(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 (v_d)_P (v_d)_N \tau P \int_A \int_A \delta(A_P - A_N)\, dA_P dA_N$$

$$\cdot \int_{E_{CN}}^{E_{VP}} \int_{E_{CN}}^{E_{VP}} \delta(E - E') \sqrt{(E_{VP} - E)(E' - E_{CN})} \cdot (f_N - f_V)\, dE dE'$$

$$= e(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \cdot (v_d)_P (v_d)_N \tau_{PA} \int_{E_{CN}}^{E_{VP}} \sqrt{(E_{VP} - E)(E - E_{CN})}\, (f_N - f_V) dE. \qquad (34)$$

Before deriving the drift velocities $(v_d)_P$ and $(v_d)_N$, we will get some idea what the τ will be. Assuming $\bar{E} = 10^5$ volts/cm,

$$\tau = \frac{h}{ae\bar{E}} = \frac{6.6 \times 10^{-27}}{3\ 10^{-8} \times 1.6 \times 10^{-12} \times 10^5} = 1.37 \times 10^{-12} \text{ sec.}$$

If we postulate that v_d is equal to the thermal velocity v_{th}, then we get $v_d \times \tau = v_{th} \times \tau = 10^8\ \ 1.4 \times 10^{-12} = 1.4 \times 10^{-4}$cm $\cong 5000 \times a$, which is not a very large distance. Therefore we may assume that the drift velocities are generated by the field $\bar{E}$ which is the same field inside of the transition region. The crudity of this assumption will be effectively compensated by taking smaller values for μ_N and μ_P (see (35)).

Then we will get

$$(v_d)_P\ (v_d)_N\ \tau = \mu_P\ \mu_N\ \bar{E}^2\ \frac{h}{ae\bar{E}} = \frac{\mu_P \mu_N h}{ae}\ \bar{E}\ . \tag{35}$$

Next, we will try to solve the energy integral

$$J = \int_{E_{CN}}^{E_{VP}} \sqrt{(E_{VP} - E)(E - E_{CN})}\ \ (f_N - f_V)\ dE\ . \tag{36}$$

Equation (36) may be normalized with respect to (kT) as follows

$$J = (kT)^2 \int_{-x_o}^{x_o} \left(\frac{1}{1 + e^{x-\mu}} - \frac{1}{1 + e^{x+\mu}} \right) \sqrt{x_o^2 - x^2}\ \ dx \tag{37}$$

where

$$x \equiv \frac{E}{kT}$$

$$x_D \equiv \frac{E_D}{kT}$$

$$x_o \equiv \frac{E_D - U/2}{kT} = x_D - \mu$$

$$\mu \equiv \frac{U}{2kT}\ .$$

Modifying equation (37), we will get

$$J = (kT)^2 \int_{-x_0}^{x_0} \frac{\sinh \mu}{\cosh \mu + \cosh x} \sqrt{x_0^2 - x^2}\ dx \quad . \tag{38}$$

Since $\frac{1}{\cosh \mu + \cosh x}$ changes its magnitude steeply at $x = \mu$, we will divide the range of x into two cases.

Case A: $\mu < x_0$ or $\mu < \frac{x_D}{2}$

$$\frac{1}{\cosh \mu + \cosh x} > \frac{2}{(1 + \cosh \mu)(1 + \cosh x)}$$

Therefore $$J \gtrsim J_1 = 2(kT)^2 \frac{x_0 \sinh \mu}{1 + \cosh \mu} \int_{-x_0}^{x_0} \frac{dx}{1 + \cosh x}$$

$$= 4(kT)^2 x_D \tanh \frac{\mu}{2} \tanh \frac{x_D}{2}$$

$$= 4(kT)^2 (x_D - \mu) \tanh \frac{\mu}{2} \tanh \frac{x_D - \mu}{2} \quad . \tag{39}$$

Case B: $\mu > x_0$ or $\mu > \frac{x_D}{2}$

$$J < J_2 = (kT)^2 \frac{\sinh \mu}{1 + \cosh \mu} \int_{-x_0}^{x_0} \sqrt{x_0^2 - x^2}\ dx$$

$$= \frac{\pi}{2} (kT)^2 \tanh \frac{\mu}{2} x_0^2$$

$$= \frac{\pi}{2} (kT)^2 (x_D - \mu)^2 \tanh \frac{\mu}{2} \quad . \tag{40}$$

Let us compare equation (39) with equation (40).

For $\mu \ll 1$, $x_D \gg 1$

$$J_1 = 2(kT)^2(x_D - \mu)\,\mu$$

$$\simeq 2(kT)^2\, x_D\mu$$

$$J_2 \simeq \frac{\pi}{4}(kT)^2(x_D - \mu)^2\mu$$

$$\simeq \frac{\pi}{4}(kT)^2\, x_D^2\,\mu$$

Therefore $$\frac{J_1}{J_2} \simeq \frac{2}{\frac{\pi}{4}x_D} \simeq 0.3$$

For $\mu \gg 1$, $x_D \gg 1$

$$J_1 \simeq 2(kT)^2(x_D - \mu)^2$$

$$J_2 \simeq \frac{\pi}{2}(kT)^2\,(x_D - \mu)^2$$

Therefore $$\frac{J_1}{J_2} = \frac{4}{\pi} \simeq 1.25$$

At $\mu = \frac{x_D}{2} > 1$

$$J_1 = 4(kT)^2\frac{x_D}{2}\tanh^2\frac{x_D}{4} = 2(kT)^2\, x_D\tanh^2\frac{x_D}{4}$$

$$J_2 = \frac{\pi}{8}(kT)^2(x_D)^2\tanh\frac{x_D}{4}$$

$$\frac{J_1}{J_2} = \frac{16}{\pi x_D}\tanh\frac{x_D}{4} \simeq \frac{16}{\pi x_D} \cong 0.5 \qquad \text{for } x_D = 10\ .$$

From this comparison we may say that J_1 and J_2 are not too far from each other.

Two approximate solutions are shown qualitatively in Figure 24. The true J lies between J_1 and J_2 as far as $u < x_D/2$.

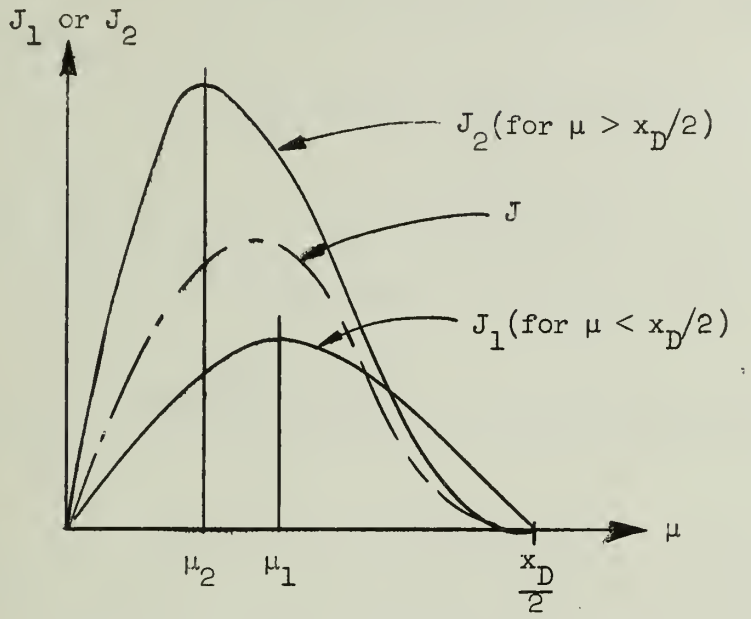


Figure 24. Approximate Solution of J

As will be seen later, the contribution of J to the RC product is rather small compared with the dominating contribution of the tunneling probability P. Therefore it does not matter which approximation form is used. The second form J_2 will be used because of its simplicity.

The peak point will be obtained as follows.

$$\sigma_2 = \frac{dJ_2}{d\mu} = 0 \qquad \text{at } \mu \simeq \mu_2 = \frac{U_2}{2kT}$$

where μ_2 satisfies

$$\sinh \mu_2 = \frac{1}{2}(x_D - \mu_2) \quad . \tag{41}$$

If $E_D = 0.15$ eV and $kT = 0.025$ eV, then $x_D = \frac{E_D}{kT} = 6$, $\mu_2 = 1.5$. This gives a valley voltage of 0.3 volts and a peak voltage of 0.075v, which are close to the values measured with germanium tunnel diodes.

The peak value of J will be

$$(J_2)_{peak} = \frac{\pi}{2}(kT)^2(x_D - \mu_2)^2 \tanh\frac{\mu_2}{2}$$

$$= \frac{\pi}{8}(2E_D - U_2)^2 \tanh\frac{U_2}{4kT} \quad . \tag{42.}$$

Since semiconductors are degenerate, E_D will not be affected by temperature. However U_2 and $(J_2)_{peak}$ are dependent on temperature, i.e., U_2 decreases and $(J_2)_{peak}$ increases as temperature decreases. This agrees to the observed tendencies.(6),(9)

A numerical example will be given in Figure 25.

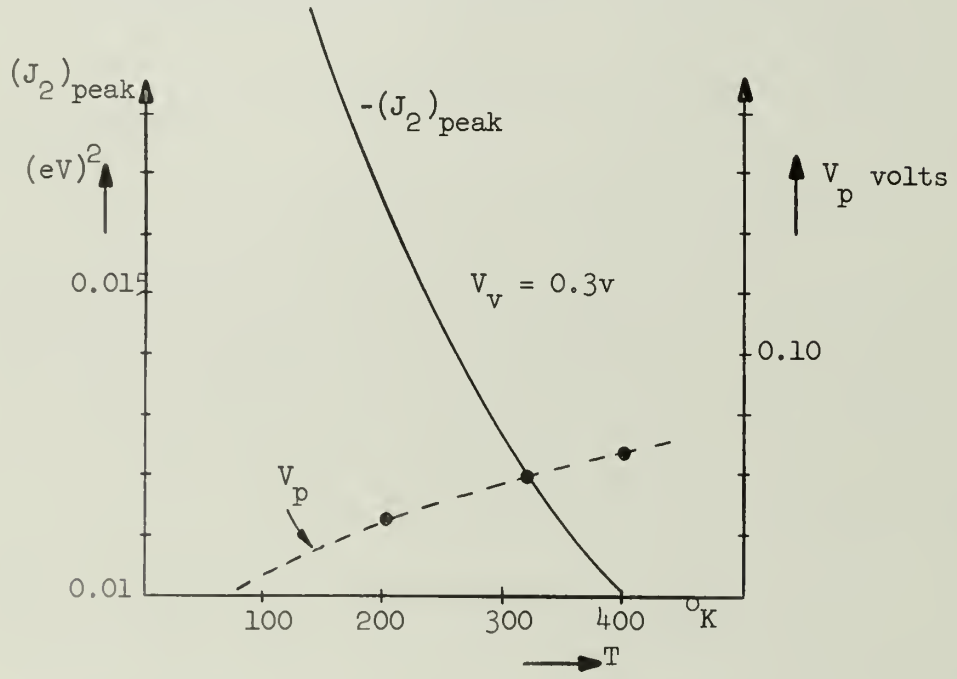


Figure 25. Temperature Dependency of J_2

The negative resistance will be calculated next. Since tunnel diodes are used in the form of diode pairs, the negative resistance at $\mu = x_D/2$ will be analyzed.

$$\sigma_2\Big]_{\mu=\frac{x_D}{2}} \triangleq \frac{dJ_2}{d\mu}\Big]_{\mu=x_D/2} = -\frac{\pi}{2}(kT)^2 x_D\left[\tanh\frac{x_D}{4} - \frac{x_D}{8}\operatorname{sech}^2\frac{x_D}{4}\right] \tag{43}$$

If $x_D/4 > 1$, (43) will be approximated by

$$\sigma_2 \Big]_{\mu=X_D/2} \simeq -\frac{\pi}{2}(kT)^2 x_D \tanh\frac{x_D}{4} \simeq -\frac{\pi}{2}(kT)^2 x_D$$

$$= -\frac{\pi}{2}(kT) E_D \quad . \tag{44}$$

From (34), (35), (41), (42) and (44)

$$I = A(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \frac{\mu_N \mu_P h}{a} P \bar{E} J \tag{45}$$

$$I_{peak} = A(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \frac{\mu_N \mu_P h}{a} P \bar{E} \frac{\pi}{8}(2E_D - U_2)^2 \tanh\frac{U_2}{4kT} \tag{46}$$

$$-G = \text{negative conductance} = \frac{dI}{dV}\Big]_{U=E_D} = \frac{dI}{du}\frac{du}{dV} = \frac{dI}{du}\frac{e}{2kT}$$

$$= -A(4\pi)^2 \left(\frac{2m_{eff}}{h^2}\right)^3 \frac{\mu_N \mu_P h}{a} P \bar{E} \frac{\pi}{4} e E_D \quad . \tag{47}$$

5.1.2 Relation to the impurity concentrations: The peak current, the valley voltage and the negative resistance have been derived using the energy level diagram. Since the impurity concentrations and the model of the junction will determine these energy levels and the built-in field in the transition region, all parameters of the tunnel diode will be expressed in terms of the number of impurity atoms per cc.

We will assume that the junction is abrupt as shown in Fig. 23 and that the concentrations of donors and acceptors are the same. Let n_D be the number of donor atoms or acceptor atoms per cm^3 and assume that they are all ionized.

From the band theory and from the abrupt junction theory, we will get

$$E_D = \frac{1}{2}\left(\frac{3}{8\pi}\right)^{2/3} \frac{h^2}{m_{eff}} (n_D)^{2/3} = 0.0313 \left(\frac{m}{m_{eff}}\right)\left(\frac{n_D}{2.5 \times 10^{19}}\right)^{2/3} eV \tag{48}$$

w = width of the transition region at equilibrium

$$= \sqrt{\frac{\epsilon}{\pi e}\ \frac{1}{n_D}\ \frac{E_G + 2E_D}{e}} = 33.5\ \left(\frac{\epsilon}{16}\right)^{1/2} \left(\frac{2.5 \times 10^{19}}{n_D}\right)^{1/2} \left(\frac{E_G + 2E_D}{1\ eV}\right)^{1/2} \text{Å} \tag{49}$$

$\bar{E}$ = field in the transition region

$$= \frac{E_G + 2E_D}{e}\Big/ w = 3\ \left(\frac{16}{\epsilon}\right)^{1/2} \left(\frac{n_D}{2.5 \times 10^{19}}\right)^{1/2} \left(\frac{E_G + 2E_D}{1\ eV}\right)^{1/2} 10^5 \text{ volts/cm} \tag{50}$$

c = transition capacity

$$= \frac{A\epsilon}{4\pi w} = 3.35\ A\left(\frac{\epsilon}{16}\right)^{1/2} \left(\frac{n_D}{2.5 \times 10^{19}}\right)^{1/2} \left(\frac{1\ eV}{E_G + 2E_D}\right)^{1/2} 10^{-7} \text{ farad} \tag{51}$$

where A is cm^2.

$$P = \exp\left[-\frac{4}{3}\ \frac{2m_{eff}}{\hbar e\bar{E}}\ (E_G)^{3/2}\right]$$

$$= \exp\left[-119\ \left(\frac{\epsilon}{16}\right)^{1/2} \left(\frac{2.5 \times 10^{19}}{n_D}\right)^{1/2} \left(\frac{1\ eV}{E_G + 2E_D}\right)^{1/2} \left(\frac{m_{eff}}{m}\right)^{1/2} \left(\frac{E_G}{0.65\ eV}\right)^{3/2}\right] \tag{52}$$

The mobilities μ_N and μ_P of degenerate semiconductors are different from that of non-degenerate semiconductors. Since there is no available measured data on germanium, we will consider $\mu_P = \mu_N$ being 1000 cm^2/volt-sec in our calculations. Then

$$I_{peak} = A \cdot 6.4 \times 10^{40} \left(\frac{m_{eff}}{m}\right)^3 \left(\frac{3\text{Å}}{a}\right) \left(\frac{\mu_N \mu_P}{10^6\ cm^4/volt^2 sec^2}\right) \left(\frac{16}{\epsilon}\right)^{1/2} \left(\frac{n_D}{2.5 \times 10^{19}}\right)^{1/2}$$

$$\times \left(\frac{E_G + 2E_D}{1\ eV}\right)^{1/2} \left(\frac{2E_D - U_2}{0.3\ eV}\right)^2 P \tanh \frac{U_2}{4kT} \text{ amp} \tag{53}$$

$$-G = -A \cdot 1.07 \times 10^{41} \left(\frac{m_{eff}}{m}\right)^3 \left(\frac{3\text{Å}}{a}\right) \left(\frac{\mu_N \mu_P}{10^6 \text{cm}^4/\text{volt}^2\text{sec}^2}\right)\left(\frac{16}{\epsilon}\right)^{1/2} \left(\frac{n_D}{2.5 \times 10^{19}}\right)^{1/2}$$

$$\times \left(\frac{E_G + 2E_D}{1 \text{ eV}}\right)^{1/2} \left(\frac{2E_D}{0.3 \text{ eV}}\right) P \quad \text{mhs} \qquad (54)$$

T = RC = inverse gain bandwidth

$$= 3.12 \times 10^{-39} \left(\frac{m}{m_{eff}}\right)^3 \left(\frac{a}{3\text{Å}}\right)\left(\frac{10^6 \text{ cm}^4/\text{volt}^2\text{sec}^2}{\mu_N \mu_P}\right)$$

$$\times \left(\frac{1 \text{ eV}}{E_G + 2E_D}\right)\left(\frac{0.3 \text{ eV}}{2E_D}\right) P^{-1} \quad \text{m}\mu\text{s} \quad . \qquad (55)$$

In Fig. 26, eqs. (53) and (55) are plotted under assumptions, that is,

$$\left(\frac{m_{eff}}{m}\right) = 1, \quad \frac{2E_D - U_2}{0.3} \tanh \frac{U_2}{4kT} = 1, \quad \frac{2E_D}{0.3} = 1, \quad \text{and } a = 3\text{Å} \ .$$

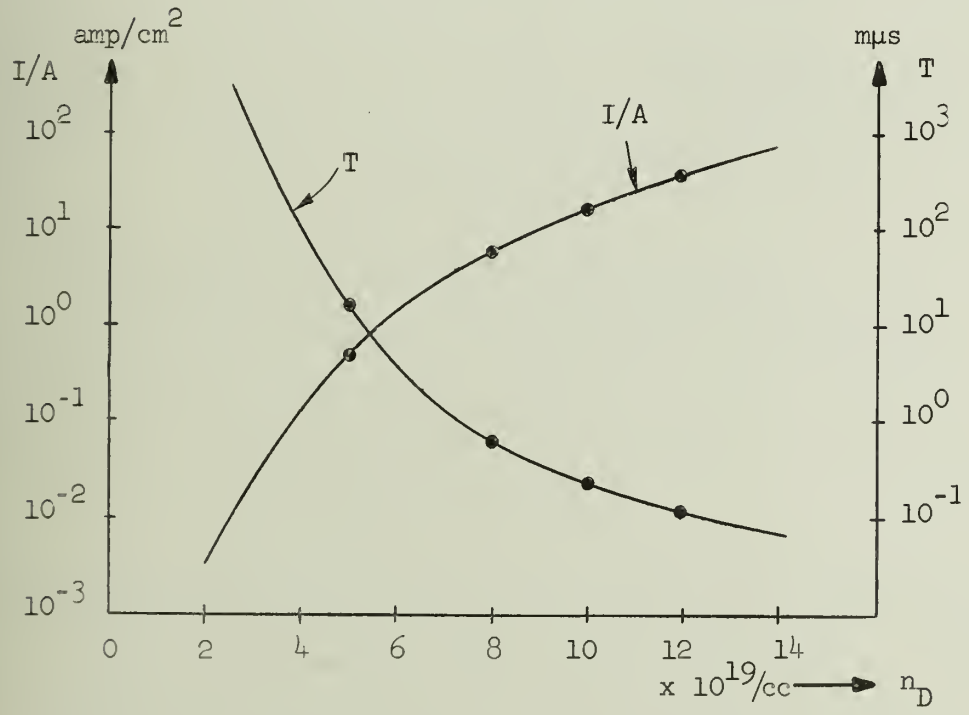


Figure 26. Impurity Level vs. Current Density and Inverse Gain Bandwidth

Any term which affects the tunneling probability has to be carefully studied because it changes greatly the numerical values obtained from the above theory. The effective mass in degenerate semiconductors is the most important factor in this sense. R. L. Batdorf et al[9] reported that faster speed was obtained by using I_nS_b which has smaller effective mass. This agrees with the above theory.

Though the model assumed in the above theory and the calculations are crude, the results will show in order of magnitude how each parameter affects the characteristics of tunnel diodes and that the very small inverse gain bandwidth will be obtained by increasing the doping level.

5.2 Inverse Gain-Band-Width of Emitter Followers

The inverse gain-band-width of emitter followers has been studied and is given as follows.[10]

$$T = \frac{1}{2\pi f_\alpha} + R_T C_c \tag{56}$$

where

f_α = alpha cutoff frequency = $\frac{\omega_\alpha}{2\pi}$

$$R_T = \frac{(R_e + r_e)(r_b' + R_b)}{R_e + r_e + r_b' + R_b}$$

R_e, R_b = external emitter, base resistance

C_c = collector depletion layer capacity including external capacities at emitter and collector .

$$\omega_\alpha \simeq \frac{2D_n}{W^2} \tag{57}$$

ω_α depends on how narrow the base width W can be manufactured.

The transistors which will be used in the system are special-purpose transistors because

(a) the signal level is extremely small ($\pm 0.2 \sim 0.3$ volts);

(b) no collector circuits are used, i.e., the collector reverse voltage is essentially constant;

(c) magnitude of current required is small;

(d) requirement of α is not severe.

Therefore W may be designed far smaller than that of regular high-level switching transistors. W can be narrowed further by making use of the space charge widening effect.

Suppose $W = 10^{-3}$ mm, which is not unrealistic (10^{-3}mm = 10^{4} Å $\cong$ 4000 germanium atoms on line!),

$$\omega_\alpha \cong \frac{90}{(10^{-4})^2} = 9 \times 10^9 = 9 \text{ KMC}.$$

R_T is essentially $r_b' \cong 100\Omega$. The effective C_c will become smaller beyond Earley's rule if a high drifting field exists in the base region (this was experimentally verified). If we assume $C_c = 1$ μμf,

$$R_T C_c = 100 \times 10^{-12} = 1.0 \times 10^{-10} .$$

Then

$$T = 1.1 \times 10^{-10} + 1.0 \times 10^{-10} = 2.1 \times 10^{-10} \text{ sec} . \qquad (58)$$

Comparing this hopeful estimate of inverse gain-band-width of transistors with that of tunnel diodes, the switching speed of a tunnel diode-emitter follower system will be transistor-limited. Under present circumstances, the situation is reversed.

$$(T)_{\text{transistor}} = 3 \times 10^{-9} \text{ sec} \qquad (T)_{\text{tunnel}} = 15 \times 10^{-9} \text{ sec} .$$

Both are measured data with one of the best transistors and tunnel diodes currently available. Anyway, as doping techniques progress and the above-mentioned special-purpose transistors are exploited, 1 nsec switching performance should be obtained without serious difficulties.

6. Basic Logical Circuits

Thus far we have investigated the general properties of tunnel diodes and their circuits and have concluded that the tunnel diode-emitter follower

combination would fulfill all of the basic requirements, namely, wave shaping, directivity and highly sensitive threshold level. As mentioned briefly at the end of Section 3, there are two ways of combining input signals, linearly or nonlinearly. The nonlinear combination is not applicable because a reset pulse is necessary. For instance, the circuit shown in Figure 27 will never change its state once it is set to the positive side ("1"). A system which uses such a basic circuit is synchronous. Inputs should be linearly combined to construct an asynchronous system. Independent diode logic is, of course, feasible.

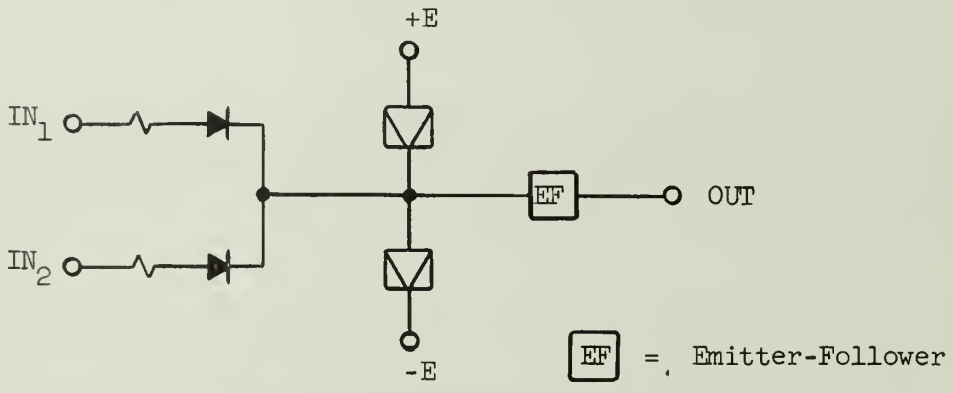


Figure 27. Nonlinear Combination which is Not Applicable

6.1 Majority Circuit

Figure 28 shows the majority circuit. The coupling resistance R_c should be

$$R_c = nR \tag{56}$$

so that

$$\frac{R_c}{n} - R = 0$$

which gives the highest sensitivity (see Section 4).

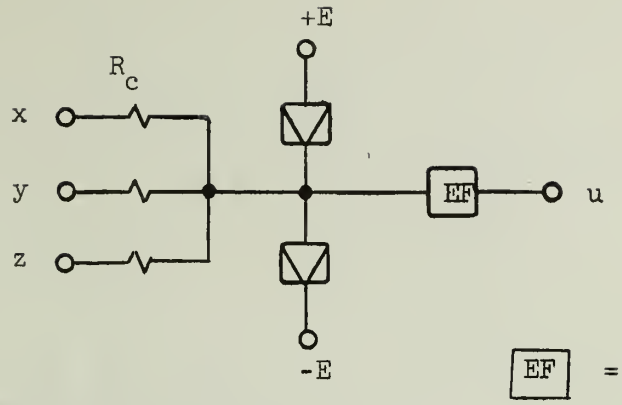


Figure 28. Majority Circuit

Let us consider the designability of the circuit because any resistor logic is supposed to have poor tolerance performance. The necessary condition is

$$V_{out} = \frac{1}{\sum R_{ci}^{-1}} \left(\sum R_{ci}^{-1} V_i\right) > \Delta V_s \tag{57}$$

or

$$\frac{v}{n}\left[1 - n\left(\frac{\Delta v}{2v} + \frac{\Delta R_c}{R_c}\right) + \frac{\Delta v}{2v}\right] > \Delta V_s$$

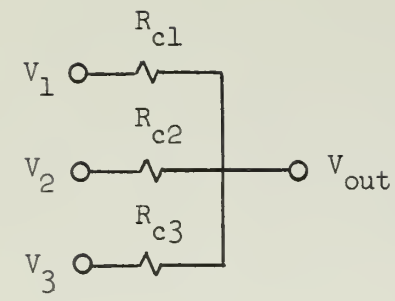
$$n < \frac{1 + \frac{\Delta v}{2v}}{\frac{\Delta v}{2v} + \frac{\Delta R_c}{R_c} + \frac{\Delta V_s}{v}} \quad . \tag{58}$$

From dc gain (14),

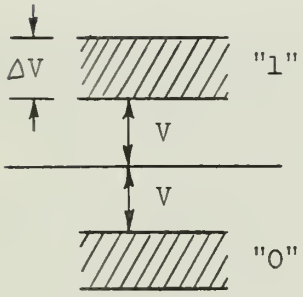
$$\frac{\Delta V_s}{v} = \Delta\left(\frac{\left|\frac{R_c}{n} - R\right|}{R}\right)_{max}$$

$$= \frac{\Delta R_c}{R_c} + \frac{\Delta R}{R}$$

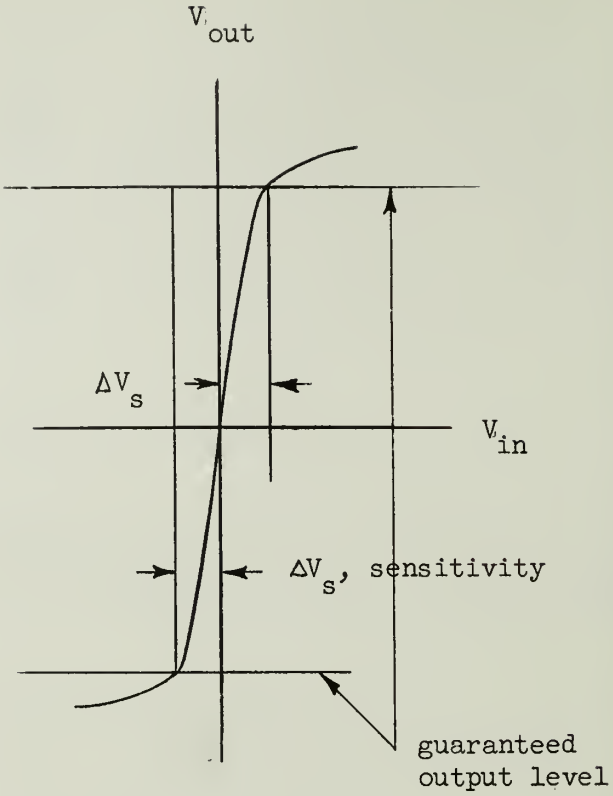
where R = negative resistance of the diode.



(a) Resistor Logic



(b) Signal Levels with their Permissible Band



(c) Wave Shaper Characteristic

Figure 29. Designability of Resistor Logic

Thus (58) becomes

$$n < \frac{1 + \frac{\Delta v}{2v}}{\frac{\Delta v}{2v} + \frac{2\Delta R_c}{R_c} + \frac{\Delta R}{R}} .$$

For the measured data with germanium diodes,

$$\Delta V = 0.02\ v \qquad v = 0.12\ v$$

$$\frac{\Delta R_c}{R_c} = 0.03 \qquad \frac{\Delta R}{R} = 0.07 \quad (150 \pm 10\Omega)$$

$$n \leq 5 .$$

Hence, the minimum number 3 for a majority element is realizable.

Tolerance conditions will be relaxed if the circuits are designed to be AND or OR circuits because the tolerance variation of fixed bias is supposed to be better than that of regular input signals.

NOTE: $u = M(x,y,1) = x \vee y$

$u = M(x,y,0) = xy$.

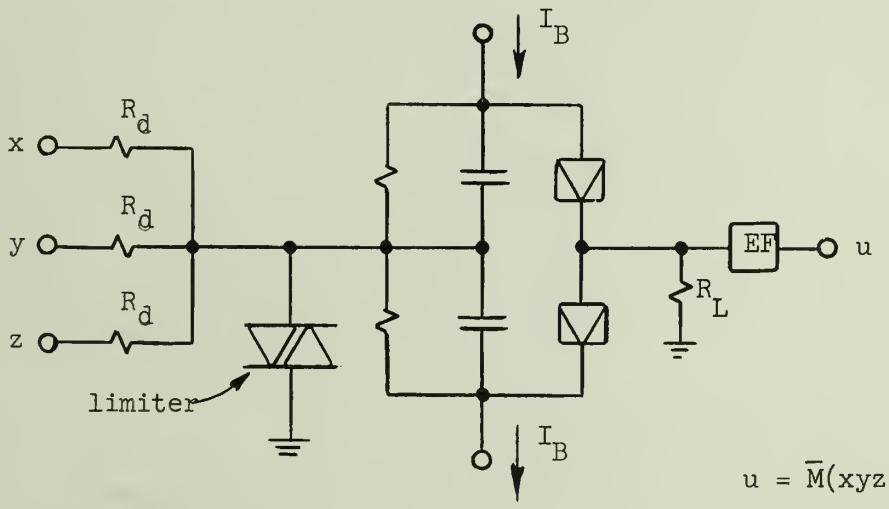
There is much to be desired for improving the uniformity of tunnel diode characteristics. The level shift of emitter-followers must be well-controlled.

6.2 Minority Circuit

Figure 30 shows the minority circuit in which a resistor logic is combined with an inverter. A limiter is inserted to limit overdriving the inverter.

NOTE: $u = \bar{M}(x,y,1) = \overline{xy}$

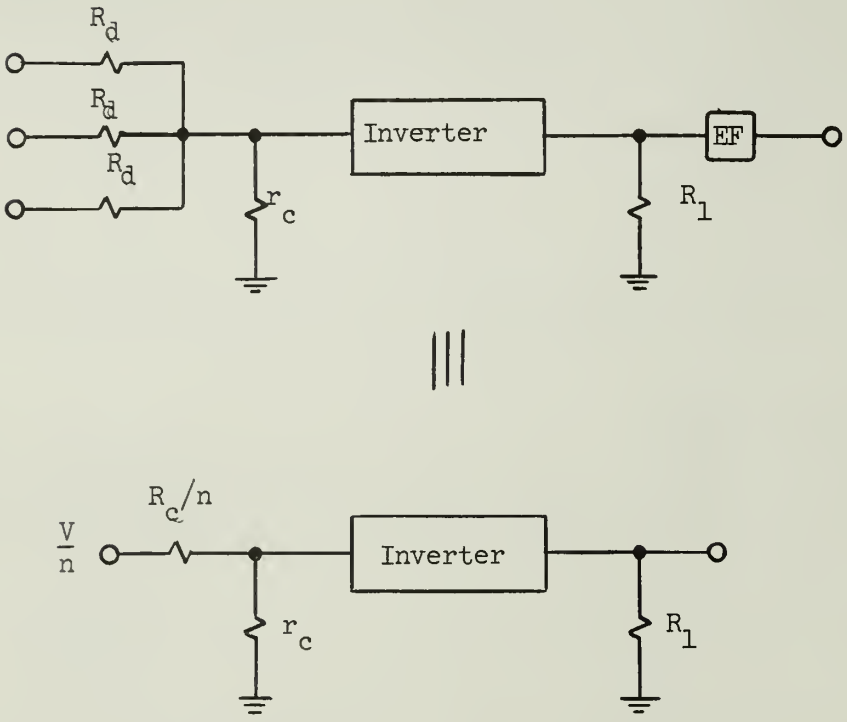
$u = \bar{M}(x,y,0) = \overline{x \vee y}$.



R_d has no relation to R. $R_L = R$

Figure 30. Minority Circuit

6.2.1 Tolerance conditions for the minority circuit:



$$\frac{V_c \frac{V}{n} \left(1 - n\left(\frac{\Delta V}{V} + \frac{\Delta R_d}{R_d}\right)\right)}{\frac{R_d}{n} + r_c} - \frac{r_c}{R_n}\left(1 + \frac{\Delta R_l}{R_n} + \frac{\Delta V}{V}\right)$$

$$> \left(\frac{\Delta R_n}{R_n} + \frac{\Delta R_l}{R_l} + \frac{\Delta V}{V}\right) V = \Delta V_s$$

$$\left(\frac{V_c}{R_d} - \frac{V_c}{R_n}\right) - \frac{V_c}{R_d}\left[n\left(\frac{\Delta V}{V}\right) + n\left(\frac{\Delta R_d}{R_d}\right)\right] - \frac{r_c}{R_n}\left(\frac{\Delta R_l}{R_n} + \frac{\Delta V}{V}\right)$$

$$> \frac{\Delta R_n}{R_n} + \frac{\Delta R_l}{R_n} + \frac{\Delta V}{V}$$

$$n + 1 < \frac{\frac{r_d}{R_n}\left(\frac{R_n}{R_d} - 1\right) - \frac{\Delta R_n}{R_n} - \frac{\Delta R_1}{R_1}\left(1 + \frac{r_d}{R_n}\right) - \frac{\Delta V}{V}\left(1 + \frac{r_d}{R_n}\right)}{\frac{r_c}{R_d}\left(\frac{\Delta V}{V} + \frac{\Delta R_d}{R_d}\right)}$$

6.3 Diode Logic

Because of the expected difficulty in tolerance requirements for resistor logic, diode logic may be introduced. Since the voltage level of junction diodes or point contact diodes does not match the voltage level of tunnel diodes, the backward tunnel diode shown in Figure 31 will be used. In the backward diode there is no forward tunneling current and the diode is practically off until the forward voltage reaches the diffusion conduction region. The circuits in which backward diode logic is combined with a restorer and an inverter are shown in Figure 32.

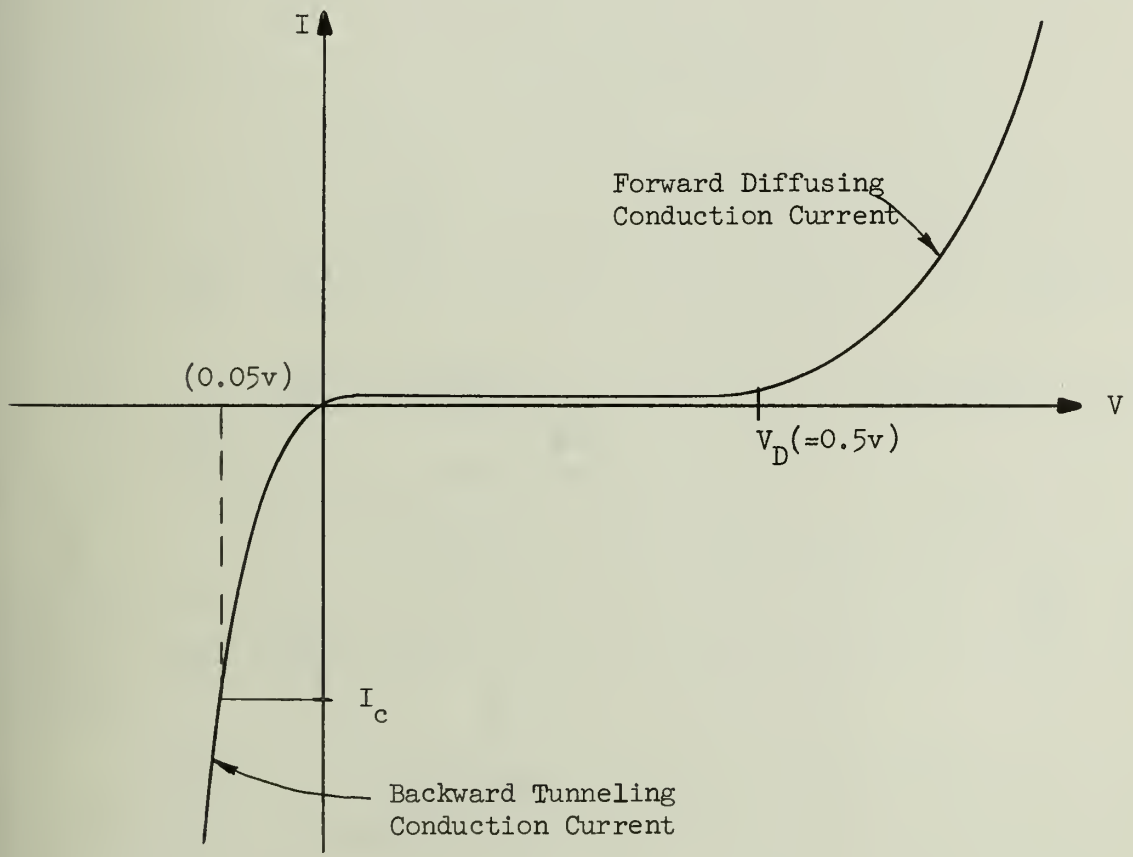
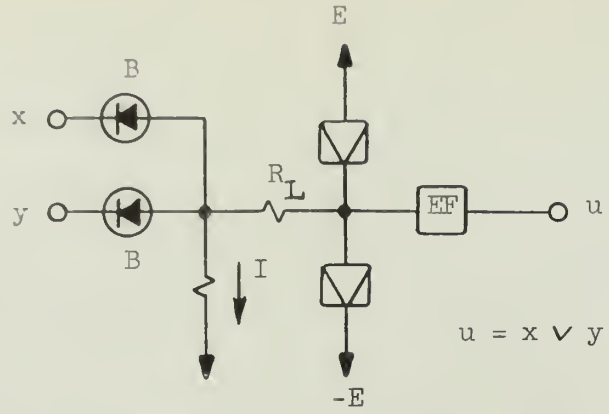


Figure 31. Characteristic of Backward Diode



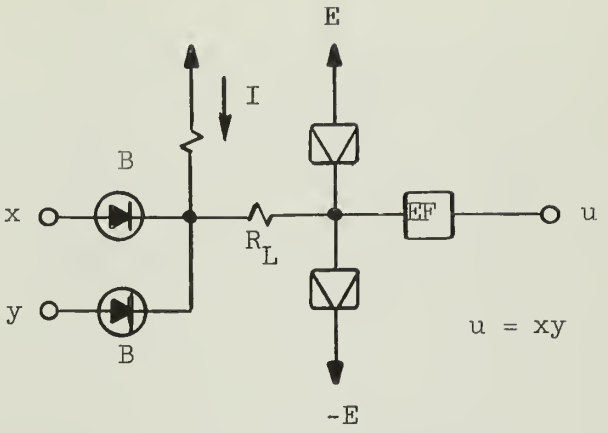
B = Backward diode $\quad I > I_m + I_c$

I_m = peak tunneling current of diode pair

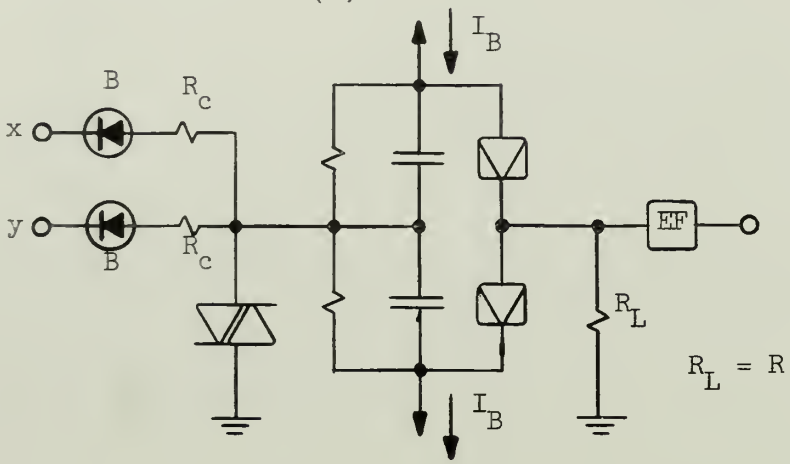
I_c = backward conduction current

$R_L = R$

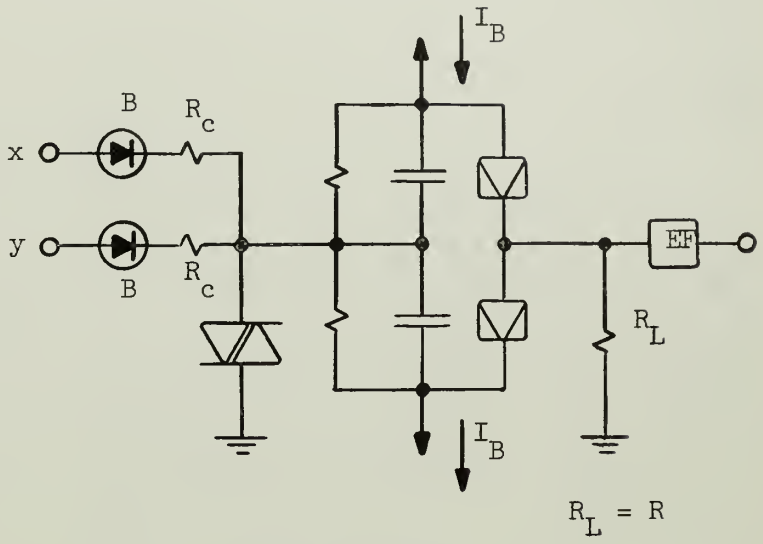
(a) OR



(b) AND



(c) OR-NOT

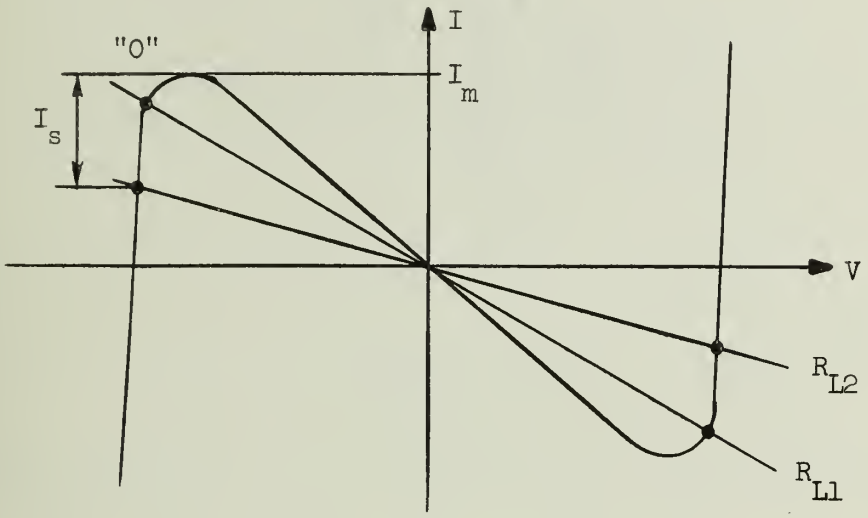


(c) AND-NOT

Figure 32. Diode Logic

6.4 AC Bias

The stability of maintaining either the "0" or the "1" state will depend upon how deeply the load line intersects the V-I curve of the diode pair (see Fig. 33). On the other hand, if R_L is increased beyond R, the



$R_{L2} > R_{L1}$, R_{L2} is more stable than R_{L1}.

Figure 33. Stability

sensitivity of the circuit will be lost. This loss can be compensated by applying ac bias of appropriate magnitude. Figure 34 is an example applied for an OR circuit. The optimum design considerations without ac bias are

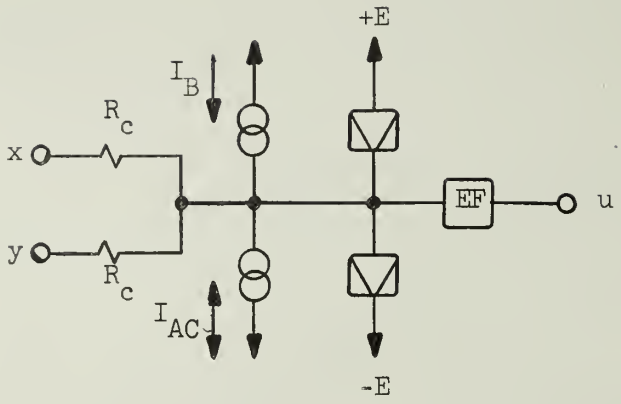
$$I_B = \frac{1}{2} I_m$$

$$R_c = 2R$$

tolerance allowance simulated for $I_m = \pm \Delta I_m = \pm \frac{1}{2} I_m$.

The optimum considerations with ac bias vary with the magnitude of the ac bias. Table 1 shows the relationship between ac bias and dc bias, stability, and tolerance.

Stability (I_s) in the sense used in this subsection will be gained for the price of more severe tolerance. The phase of ac bias does not need to be controlled. The ac bias scheme will be applied in diode logic more



$\frac{R_c}{2} > R$

Figure 34. OR with AC Bias

Table 1. Stability and AC Bias

I_{AC}	0	$\frac{1}{3} I_m$	$\frac{1}{2} I_m$	$\frac{3}{5} I_m$
I_B	$\frac{1}{2} I_m$	$\frac{1}{3} I_m$	$\frac{1}{4} I_m$	$\frac{1}{5} I_m$
$\pm \Delta I_m$	$\pm \frac{1}{2} I_m$	$\pm \frac{1}{3} I_m$	$\pm \frac{1}{4} I_m$	$\pm \frac{1}{5} I_m$
R_c	2R	3R	4R	5R
I_s	$\frac{1}{2} I_m$	$\frac{2}{3} I_m$	$\frac{3}{4} I_m$	$\frac{4}{5} I_m$

successfully (Fig. 35). If the characteristic of the backward diodes is perfect, $\pm$ 100% variation of I_m is allowable.

An EXCLUSIVE OR circuit using two-wire logic, ac bias, and single diodes (not diode pairs) was constructed and operated up to 6 mc. The RC product of the diodes (Fairchild) was about 100 nsec. Therefore we may conclude that the frequency of ac bias will be about equal to 1/RC cycle. If the frequency f is smaller than this, 1/f will be the switching speed of the system, that is the speed of the system is controlled by the ac bias but not by the inverse gain-band-width of the tunnel diodes.

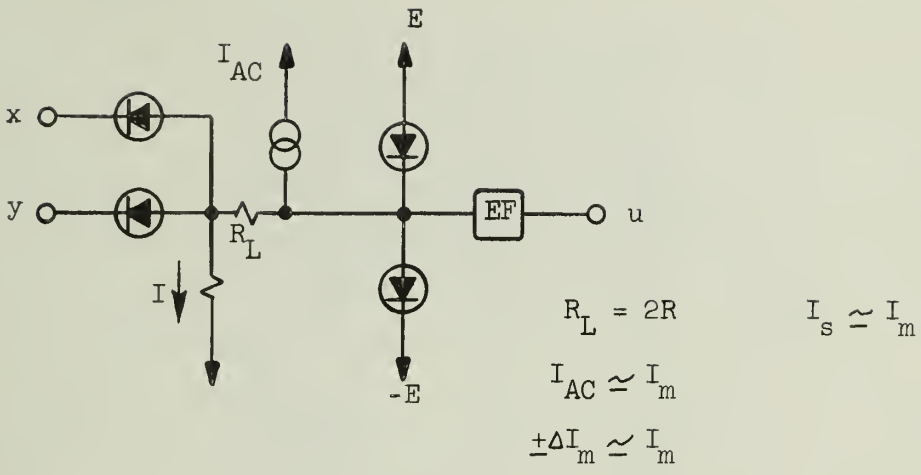


Figure 35. OR with AC BIAS

6.5 Flipflop

A Schmitt trigger, both in-phase and inverse-phase, will be obtained simply by designing $R_L > R$ in wave shapers. A symmetric flipflop is shown in Figure 36. (See page 52.)

Using a majority function, a C-element which functions

$$C' = xy \vee (x \vee y)\, C$$

will be obtained by the circuit shown in Figure 37.

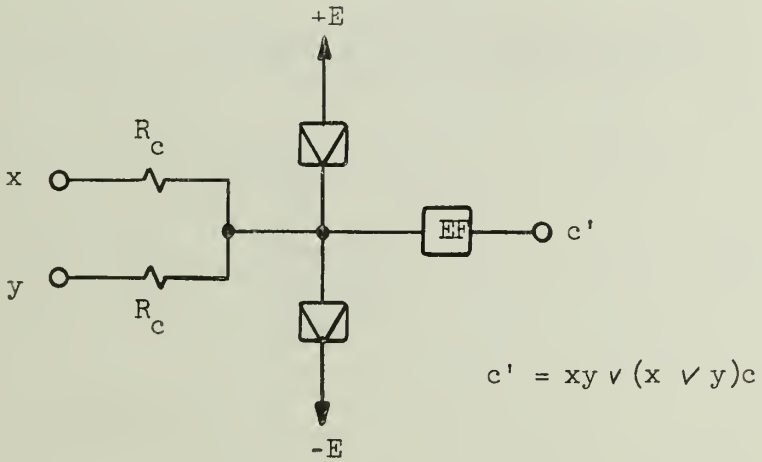
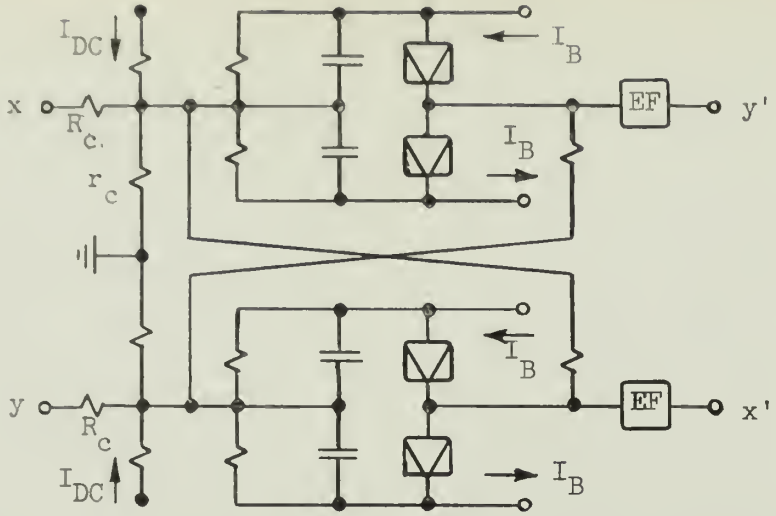
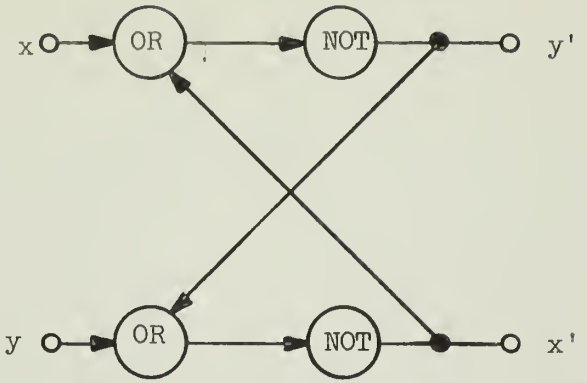


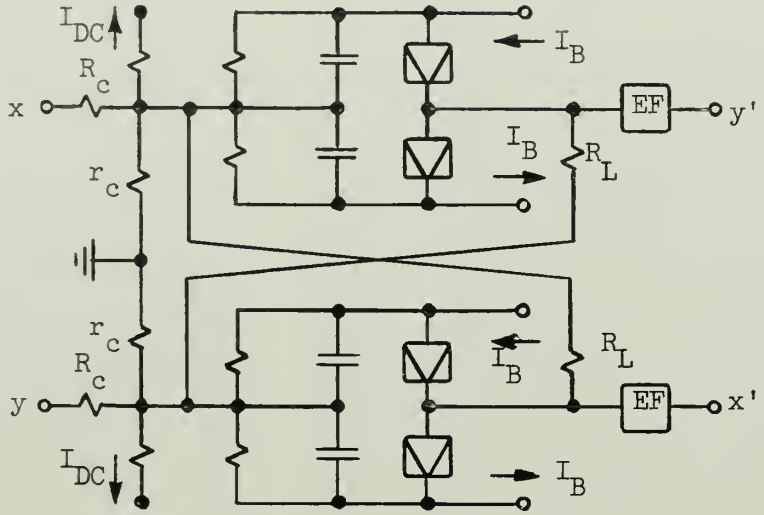
Figure 37. C-element



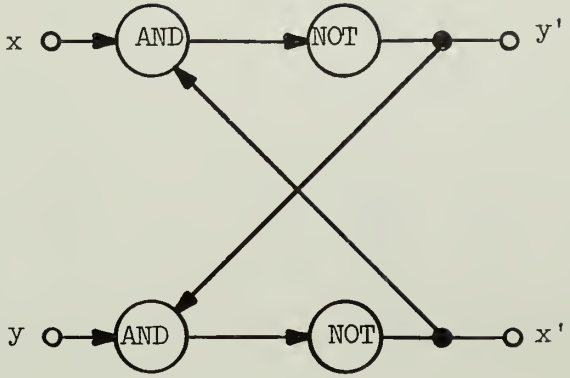
(a) Symmetric Flipflop



(b) Logical Equivalent to (a)



(c) Symmetric Flipflop



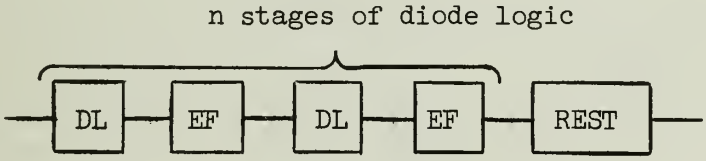
(d) Logical Equivalent to (c)

Figure 36. Symmetric Flipflop

7. Miscellaneous Applications

7.1 Level Shift Compensator

Signal levels will be shifted down after passing several stages of diode logic - emitter followers. A restoring circuit is required to re-establish the signal level after passing a certain number of stages of diode logic. Unfortunately, the restoring circuit is one of the most time-consuming circuits in this type of system. If the restoring circuit is eliminated from the system, the over-all speed will be improved. The magnitude of level shift caused by each diode logic - emitter follower stage is very small, $\pm$ 0.2 $\sim$ 0.3 volts usually.



A tunnel diode circuit was designed to compensate this level shift (Fig. 38). When u_{in} is positive, T_1 is in the low voltage - high current

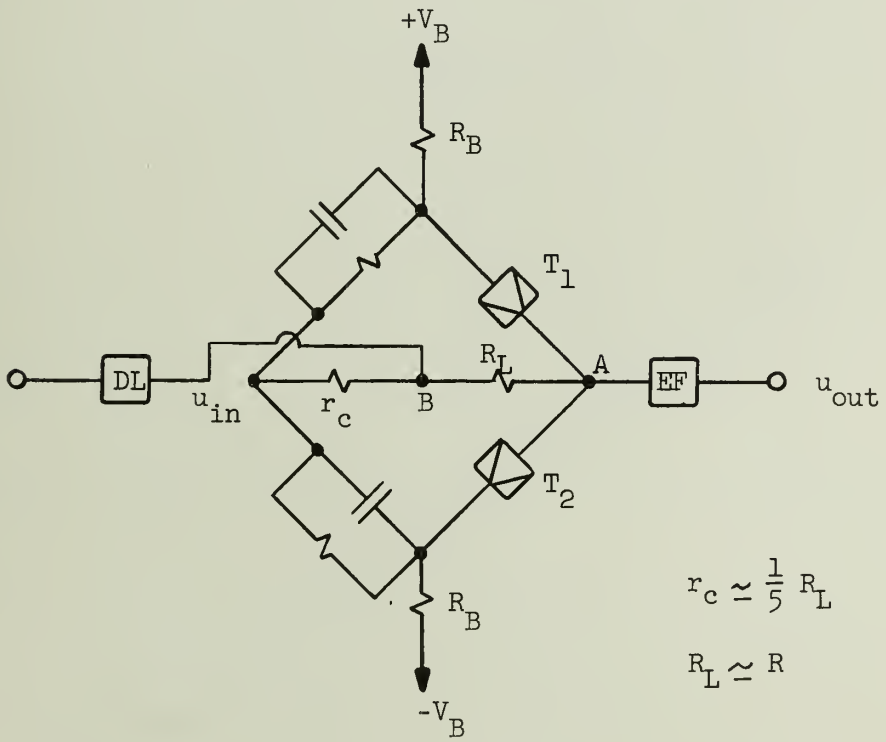
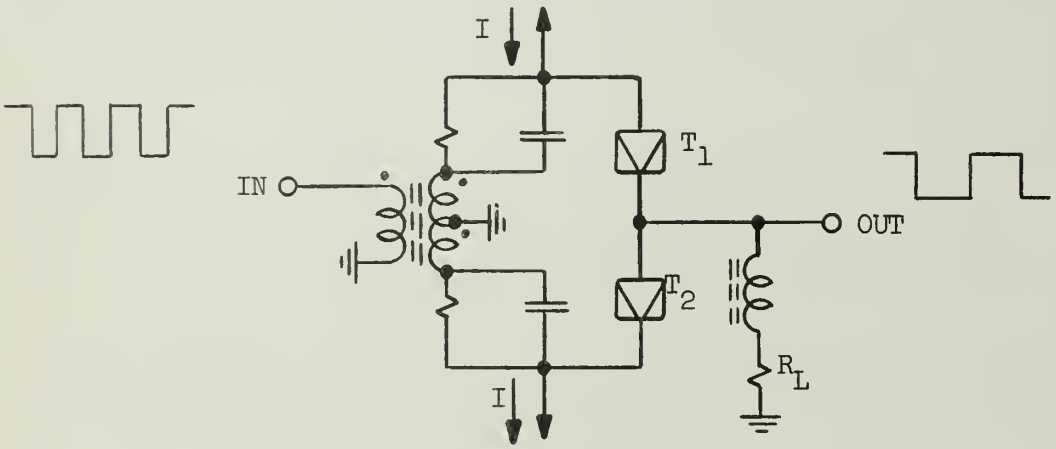


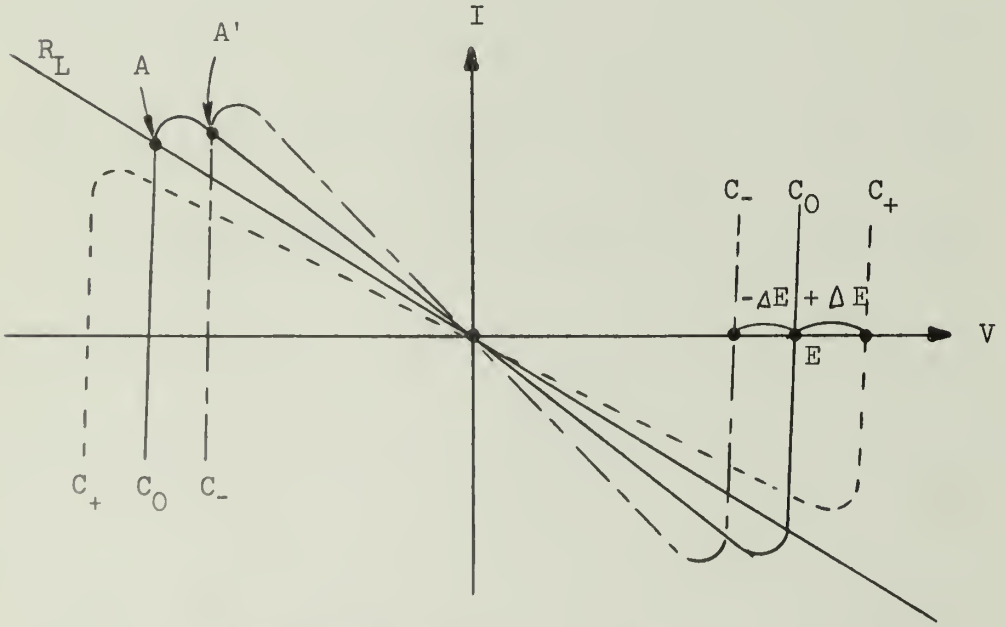
Figure 38. Level Shift Compensator

state and T_2 is in the high voltage - low current state. The unbalanced current will flow from A to B in Fig. 38 thus developing an assisting voltage across R_L in series with u_{in}. The reverse is true for negative input. If, for instance, $G_a A_s$ tunnel diodes are utilized, the voltage across R_L is about 0.3 volts, which is sufficient to compensate for the lost amplitude at each stage of diode logic - emitter follower.

7.2 Scale-of-Two Counter



(a) Counter



(b) Graphical Analysis of Counter

Figure 39. Scale-of-Two Counter

Consider the circuit shown in Figure 39(a). The load resistance R_L of the diode pair is chosen to be larger than the negative resistance R of the diode pair. There are two stable states in the circuit. A negative going input will induce voltages ΔE across the secondary winding such that the effective bias voltage of the diode pair is $E - \Delta E$. Therefore the V-I curve of the diode pair is now shifted from C_0 to C_-; however the state of the circuit will not change. For example, the state A on the C_0 curve will be shifted to the state A' on C_-; thus the output voltage may be a little smaller than A but the state remains the same. A positive going input will change the bias from E to $E + \Delta E$; thus the V-I curve is shifted from C_0 to C_+.

If the bias is sufficiently modulated, the negative resistance will become larger than R_L and the circuit will become unstable. The current tends to be zero. During this process the induced voltage on L affects differentially T_1 and T_2 in such a way that the change of the state of the diode is assisted. If the positive going input is terminated when this change of the state is completed, the circuit will stay stably in its new state. This process will be taken at every positive going edge of the input pulses; thus the circuit will perform as a differential counter. The circuit seems to be similar to the circuit reported by W. F. Chow[11]. Fig. 40 shows an actual circuit using Ge tunnel diodes and the observed waveforms are shown in Figure 41. (Fig. 40 will be found on page 56, Fig. 41 on page 57.)

The stored energy in the inductance L should be just enough to change the state of the circuit. If it is too large, the counting speed will be slow. The circuit shown in Fig. 40 is capable of counting 15 mc sinusoidal input.

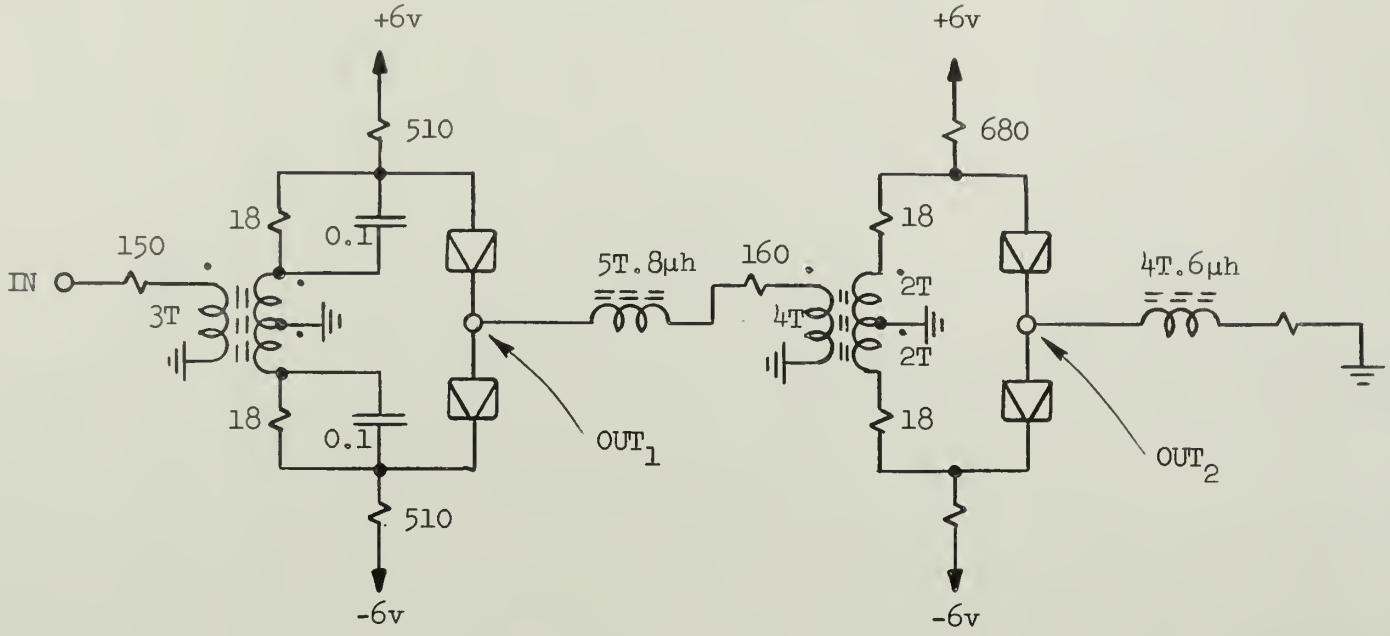


Figure 40. Practical Circuit of Scale-of-Two-Counter

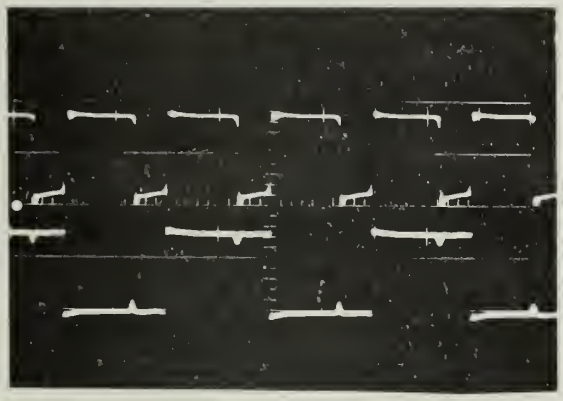


Figure 41. Waveforms of the Counter

8. Conclusions

Asynchronous circuits using tunnel diodes were investigated and feasibility of the circuits was clarified. Some experimental data were obtained. Since tunnel diodes are not carrier band devices but base band devices in their nature, the study of constructing asynchronous systems should be as successful as the study of synchronous systems. An attempt was made to design a memory array of tunnel diodes. The result was so insignificant in its effect on the characteristics of the diodes that it was not included here. Further study is needed.

The author is grateful to Professor W. J. Poppelbaum and his colleagues for their helpful suggestions and their supplying of precious tunnel diode samples for this work.

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